An accurate BJT-based CMOS temperature sensor with Duty-Cycle-Modulated output

Abstract—This paper describes the design of a precision BJT-based temperature sensor implemented in a standard 0.7µm CMOS process. It employs parasitic PNPs as sensing elements, and so is insensitive to mechanical (packaging) stress. The PNPs are readout by a duty-cycle modulator, whose quasi-digital output can easily be interfaced to the digital world and, by low-pass filtering, to the analog world as well. A chopping and Dynamic Element Matching (DEM) scheme averages the effects of amplifier offset and component mismatch over 8 cycles of the modulator's output, after a single-temperature trim, result in an accuracy of ±0.1°C (-20°C to 70°C) and ±0.3°C (-45°C to 130°C). Measurements of sensors packaged in TO-18, TO-92 and TO-220 show that the resulting packaging shift is less than 0.1°C. Measurements of 8 sensors over 72 days show the output variation is less than 2.5mK. The sensor also achieves state-of-the-art energy efficiency, having a resolution of 3mK (rms) resolution in a measurement time of 1.8ms, while dissipating only 200µW. A single measurement consumes only 356nJ. This combination of high accuracy, high resolution, high speed and low energy consumption makes this sensor well suited for commercial and industrial applications.

Index terms – CMOS temperature sensor, Duty-cycle-modulation, Chopping, Dynamic Element Matching (DEM), One-point trim.

I. INTRODUCTIE

SMART temperature sensors based on the combination of Bipolar Junction Transistors (BJTs) as sensing elements and a duty-cycle modulator as readout circuit have been commercially available since 1989 [1]. Compared to the more widely used sigma-delta modulators, an attractive feature of duty-cycle modulators is that they can easily and robustly be connected to digital systems, such as microcontrollers, as well as to analog systems, such as thermostats. In addition to being simple and power efficient, duty-cycle modulators can be readily designed to be insensitive to typical circuit non-idealities such as offset and component tolerances.

Previous sensors, such as those presented in [1] and [2], exploited the benefits of bipolar or BiCMOS technology, e.g. good component matching and the availability of high-performance BJTs, to achieve good accuracy. Compared to CMOS technology, however, these benefits came at the expense of somewhat higher manufacturing cost. Although the analog performance of CMOS technology is arguably poorer, later work has demonstrated that it can also be used to realize accurate temperature sensors [3] - [7]. The CMOS temperature sensors typically employ dynamic error-correction techniques, such as chopping, correlated-double sampling and Dynamic Element Matching (DEM) to mitigate the effects of component mismatch, and employ compensation schemes to mitigate the effects of the low current gain of the substrate PNPs available in CMOS technology [3][8]. Rather fortuitously, such PNPs turn out to be quite insensitive to the mechanical stress induced by packaging [9]-[11].

This paper describes a precision CMOS temperature sensor that was designed to be a backward-compatible version of the BiCMOS sensor described in [1] and its predecessor in bipolar technology [2]. It improves on its predecessors by combining higher accuracy, higher resolution and lower power dissipation with lower fabrication cost. The sensor employs a continuous-time duty-cycle modulator whose system-level design is described in Section 2. This is followed, in Section 3, by a description of a self-clocked chopping and DEM scheme that averages component mismatch over 8 cycles of the modulator's output. Details about the circuit implementation and signal processing are presented in Section 4 and 5, respectively. Measurement results are described in Section 6.

II. BASIC DESIGN

For compatibility, the basic operation of the CMOS temperature sensor (Fig. 1) is chosen to be the same as that of the predeceasing designs [1] and [2]. Under the control of a Schmitt trigger (ST), a capacitor C is consecutively charged by a current I_1 up to a threshold voltage V_2 and then discharged by a current I_2 down to a threshold voltage V_1 (Fig. 1 (a)). As can be deduced from the timing diagram shown in Fig. 1 (b), the duty-cycle D of the resulting relaxation oscillation is then given by:

$$D = \frac{t_H}{t_L+t_H} = \frac{\frac{(V_2-V_1)C}{I_2}}{\frac{(V_2-V_1)C}{I_1}+\frac{(V_2-V_1)C}{I_2}} = \frac{I_1}{I_1+I_2} \quad (1)$$

It should be noted that the value of D is independent of the exact value of the ST's threshold voltages V_1 and V_2 and of the capacitance C. The two currents I_1 and I_2 are designed to be temperature dependent: I_1 is linearly proportional to absolute temperature (PTAT), while I_2 is complementary-to-absolute-temperature (CTAT) (Fig. 1 (c)). Furthermore, if the sum $I_{ref} = I_1+I_2$ is designed to be temperature independent (as indicated in Fig. 1 (c)), then D will be a linear function of temperature. In a CMOS process, I_2 can be derived from the base-emitter

voltage V_{BE} of a substrate PNP, while I_1 can be derived from the difference ΔV_{BE} between the base-emitter voltages of two appropriately biased PNPs. However, as shown in Fig. 1(c), the resulting duty-cycle D will then vary by only about 30% over the desired temperature range: -45°C to 130°C.

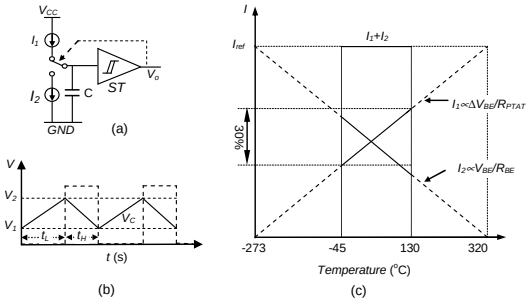

Fig. 1. The operation principle of the temperature sensor. (a) Basic principle; (b) the voltage across the capacitor C; (c) various (extrapolated) currents as a function of temperature.

To increase the dynamic range of D, the currents I_1 and I_2 can be implemented as the combination of a PTAT current and a CTAT current [2], such that $I_1 = 3I_{PTAT} - 0.5I_{CTAT}$ and $I_2 = I_{CTAT} - I_{PTAT}$. As in [2], the sum of the charging and discharging currents, i.e. $2I_{PTAT}+0.5I_{CTAT}$, was designed to have a slightly positive temperature coefficient, which effectively compensates for the curvature in V_{BE3}. As shown in Fig. 2, this scheme ensures that D now varies from about 10% to 90% over the desired temperature range: –45°C to 130°C.

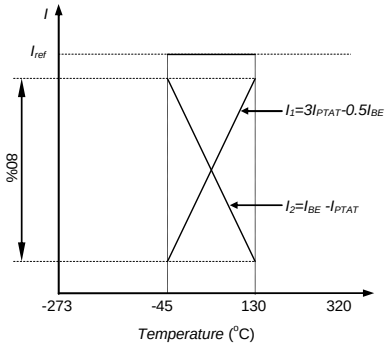

Fig. 2. The charge and discharge current in this design.

Fig. 3 shows a simplified block diagram of the actual CMOS sensor. Substrate bipolar PNP transistors Q_1 and Q_2 are biased at a 1:9 current-density ratio, and an Op-amp (OP_1) forces the resulting voltage $\Delta V_{BE}=(kT/q)\ln(9)$ across a resistor R_{PTAT} to generate a PTAT current $I_{PTAT}=\Delta V_{BE}/R_{PTAT}$ (~1µA at room temperature). Similarly, OP_2 and another resistor R_{BE} convert the base-emitter voltage V_{BE3} of Q_3 into a CTAT current $I_{CTAT}=V_{BE3}/R_{BE}$. Next, these currents are linearly combined such that the capacitor C is charged by a current $I_1=3I_{PTAT}-0.5I_{CTAT}$ and is discharged by a current $I_2=I_{CTAT}-I_{PTAT}$.

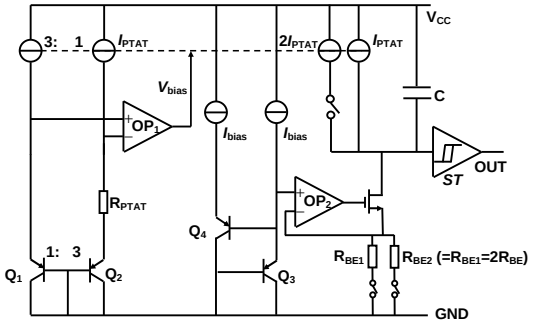

Fig. 3. The principle schematic circuit.

By properly choosing the values of R_{PTAT} and R_{BE}, as well as the nominal value of V_{BE3}, a linear duty-cycle versus temperature characteristic can be realized:

$$D = a_0 + a_1 \vartheta \qquad (2)$$

where ϑ is the temperature in degree Celsius. For compatibility with the previous design [1], the sensor was designed such that $a_0 = 0.32$ and $a_1 = 0.0047(^oC)^{-1}$.

III. Design For Accuracy

An important error source is component mismatch, which causes the ratios between the various charging and discharging currents to spread. In order to minimize this, the ratio R_{BE}/R_{PTAT} is set by using large devices and careful layout, while the effects of op-amp offset and 1/f noise are mitigated by chopping. Errors in the ratios of the currents of current-mirrors and resistances, as well as in the ratio of the emitter areas of the substrate PNPs are mitigated by Dynamic Element Matching (DEM). Since the DEM switches used to interchange Q_1 and Q_2 cause some voltage drop, Kelvin connections are used to accurately sense ΔV_{BE} [6] [12]. The DEM and chopping-state machines are self-clocked (by the output of the Schmitt trigger), and so no external clock is required.

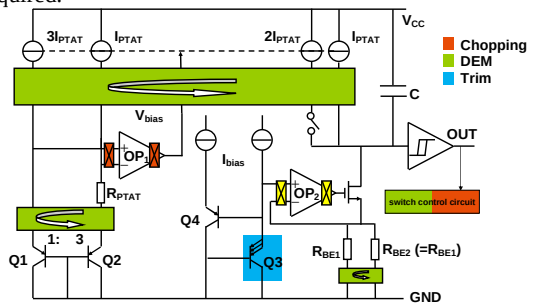

Fig. 4. Circuit modifications for reaching a higher accuracy.

According to the circuit shown in Fig. 4, seven identical PTAT current sources are used to bias Q_1 and Q_2, as well as to charge and discharge the capacitor C. Therefore, a DEM cycle with at least seven states is required. Furthermore, four identical PNP transistors Q_1 and Q_2 were used to realize an emitter ratio of three. A complete DEM cycle of these transistors thus requires four steps. Lastly, the op-amps need to be chopped and the nominally identical R_{BE} resistors need to be swapped. To satisfy all these requirements, an extra dummy current source was added to the circuit (not shown in

Fig. 4) and a DEM cycle with eight states was chosen. During each DEM cycle the following actions take place:

- the current sources are rotated once,
- the four BJTs are rotated twice,
- the R_{BE} resistors are swapped four times,
- the Op-amps are chopped four times.

Averaging the duty cycles of eight periods reduces the errors caused by component mismatch to second order. Rotating all four groups of components simultaneously means that not all possible permutations of their locations are implemented, thus significantly reducing the required number of DEM states. However, for this to work well, the various error sources should be independent. This was confirmed by simulations, which show that the chosen simplified approach doesn't degrade accuracy, since the most dominant source of error is due to the offset of op-amp OP1.

Another important error source is due to the effect of process spread in V_{BE3} [2], in the selected CMOS technology, this amounts to a maximum of about ±15mV, which corresponds to about ±4°C temperature error. This can be corrected by trimming both the bias current and the emitter area of Q_3. The required trimming range is about 10°C, where the spread of resistances has also been taken into account. The worst-case trimming step is about 50mK. Another source of error and spread is due to the finite current gain β of the substrate PNPs (about 25 at room temperature). As shown in Fig. 4, an extra current source (not included in the DEM scheme) and a substrate PNP (Q_4) are used to implement a simple beta-compensation scheme.

IV. Circuit Design

In this section, some key aspects of the circuit level implementation of the CMOS temperature sensor will be presented.

A. Current mirrors and current sources

A wide-swing cascoded current mirror [13] was used to generate the PTAT currents (Fig. 4). Its large output impedance ensures that I_{PTAT} remains constant during the charging and discharging of the modulator's timing capacitor C. This ensures that the sensor has a low supply-voltage sensitivity.

B. Op-amps

The finite gain of OP_1 and OP_2 causes errors in I_{PTAT} and I_{CTAT}, respectively. In order to keep the resulting temperature-sensor errors below, for instance, 50mK, the gains of OP_1 and OP_2, must be larger than 90dB and 70dB, respectively. Moreover, they must be able to handle input voltages (V_{BE}) down to about 0.3V at 130°C. Both requirements were met by implementing OP_1 and OP_2 as folded-cascode amplifiers with PMOS input pairs [14].

C. Schmitt trigger

As shown in Fig. 5, the Schmitt Trigger (ST) is based on the use of two inverters in series, with a positive feedback path that controls the threshold voltages of the first inverter [15]. When the ST's output is HIGH, M_1 is bypassed by M_6, and so its lower threshold (V_1 in Fig. 1 (b)) will be set by the threshold voltage of M_2, i.e. V_{TH2}. When its output is LOW, M_4 is bypassed by M_5, and so its upper threshold voltage (V_2 in in Fig. 1 (b)) will be close to V_{CC} - $|V_{TH3}|$. The amount of positive feedback is determined by the relative W/L ratios of $M_{2,3}$ and $M_{1,4}$. The large voltage swing range (about V_{CC} – 2V) at the input of the ST ensures that its input-referred noise has negligible impact on the duty-cycle. By using a large capacitor (C ~150pF), the modulator's oscillation frequency is designed to be low enough (less than 7kHz) to ensure that the error caused by the ST's own switching time (a few nanoseconds) is less than 10mK.

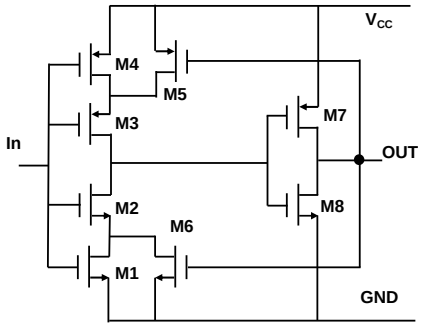

Fig. 5. The schematic circuit of Schmitt trigger.

D. Calibration

An 8-bit trimming network, consisting of a switchable array of PNPs, was used to adjust the base-emitter voltage of Q_3 (in Fig. 4) and compensate for process spread. The base-emitter voltage can be trimmed within a range of 0mV to 40mV, which varies in a non-linear manner with a worst case resolution of about 50mK. After calibration, the trim code is stored by zapping Zener diodes, which form a reliable and low-cost form of on-chip memory.

V. Signal Averaging

As discussed in Section 3, errors due to component mismatch and offset are averaged over eight successive periods of the duty-cycle modulator, i.e. over a full DEM cycle. There are various way of averaging, as will be discussed now.

Fig. 6 shows the output signal of the temperature sensor over a full DEM cycle. A microcontroller can measure the time intervals t_{L1}, t_{H1}; t_{L2}, t_{H2}; etc. A first method is to compute the duty-cycle of each period and then to average the results to obtain D_{avg1} as:

$$D_{avg1} = \sum_1^8 (t_{Hi}/(t_{Hi}+t_{Li}))/8 \quad (3)$$

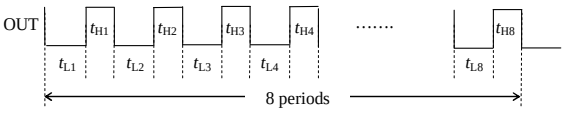

Fig. 6. The output signal of the temperature sensor.

A simpler method, which involves only a single division, is to sum the "High" and "Low" intervals and compute D_{avg2} as follows:

$$D_{avg2} = \sum_1^8 t_{Hi} / \sum_1^8 (t_{Hi} + t_{Li}) \quad (4)$$

This second way of averaging is equivalent to applying an analog low-pass filter to the modulator's output. applying an analog low-pass filter can convert the duty cycle output to a DC signal, which can easily be read by for instance a multi-meter, or be directly used in an analog temperature-control system [17]. However, it does not completely cancel the mismatch-induced errors. Fig. 7 shows the simulated residual temperature error caused by 1mV offset in OP_1 (Fig. 4) for the two averages D_{avg1} and D_{avg2}, respectively. Note that the latter way of averaging results in more error, especially at low temperatures. However, for the limited range of -10 °C to + 110 °C, the error is still less than 0.1 °C, which is acceptable in many applications.

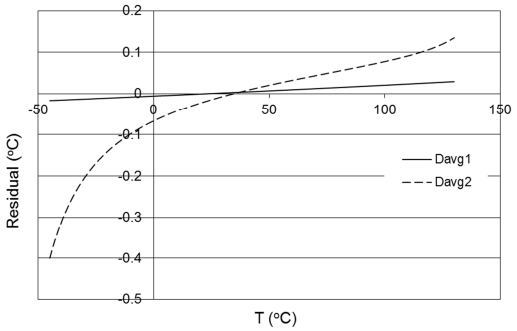

Fig. 7. Simulated residual errors obtained with D_{avg1} and D_{avg2} for an offset voltage V_{os1} = 1mV of OP_1.

Better temperature-sensing resolution can be obtained by averaging the sensor's output over more than one DEM cycle. In that case, a third way of averaging can be applied to reduce the number of divisions required, while still obtaining high accuracy. This involves calculating the duty-cycle D_{avg3} as follows:

a) Suppose that the numbers N_{L1}, N_{H1}, N_{L2}, N_{H2}, … N_{L8}, N_{H8}, counted by a microcontroller with its internal clock frequency, represent the 16 time intervals t_{L1}, t_{H1}; … t_{L8}, t_{H8} of the sensor's output over one DEM cycle.
b) For the first 8 periods, the values of N_{L1} to N_{H8} are stored in separate registers.
c) For the 9th period (= the first period of the second DEM cycle), the number N_{L9} corresponding to its LOW interval is added to N_{L1}, while the number N_{H9} is added to N_{H1}. In a similar manner, this is done for the other 14 time intervals of the second DEM cycle.
d) Step c) is repeated for all other DEM cycles.
e) Next, the duty cycle D_{avg3} is calculated with an equation similar to Eq. (3):

$$D_{avg3} = \sum_1^8 (N_{Hi}/(N_{Hi}+N_{Li}))/8 \quad (5)$$

Note that for M DEM cycles only eight divisions are performed. So, as compared to using D_{avg1}, this approach reduces the calculation time by roughly a factor M. Its accuracy is essentially the same as that of D_{avg1}.

VI. Fabrication and Test Reculs

The temperature sensor was fabricated in 0.7µm CMOS technology (Fig. 8). The die size is 1.7mm x1.3mm. In total, the chip has 13 pads. Nine of them are used to store the trimming code determined by a wafer-level calibration at room temperature. The other four pads are available to the user and are: V_{CC}, GND, OUT and PD (an optional pad).

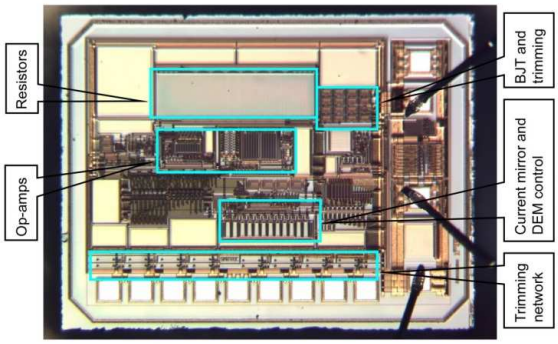

Fig. 8. Chip photo of the temperature sensor.

A. DEM and averaging

The sensor's output is a rail-to-rail square wave, whose frequency varies from about 500Hz to 7kHz and is supply and temperature dependent. For an accurate result, the duty-cycle of 8 successive periods must be averaged in one of the ways described in section 5. The temperature can then be calculated using Eq. 2. To determine the temperature sensor's error, its output was compared to that of a reference sensor, (a platinum resistor Pt100 calibrated to within ±20mK). Care has been taken to ensure that the temperature difference between the sensor and the reference sensor is less than 10mK.

Fig. 9 shows the real-time measurement results for each period (blue line: without any averaging) together with the moving average, using Eq.3, over eight periods (pink line). The results repeat every eight readings, corresponding to the eight states of one DEM cycle. The standard deviations before and after averaging are 2.7°C and 3mK, respectively. So, by taking the average of a complete DEM cycle (eight periods), the error caused by component mismatch is reduced by almost a factor 1000! Note that the measurement can be started at an arbitrary transient in a DEM cycle. So no synchronization is required because any series of eight periods will cover a full DEM cycle.

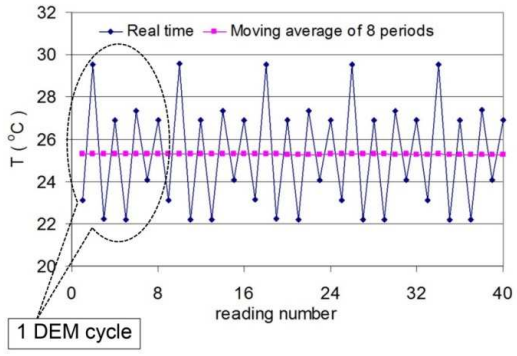

Fig. 9. Measured temperature reading at room temperature.

B. *Accuracy versus temperature*

To characterize device spread, 36 calibrated samples in metal TO-18 package were tested over the temperature range from -45°C to 130°C. Fig. 10 shows the measured temperature error after computing the average duty cycle from Eq. 3 (D_{avg1}). This figure shows clearly the systematic nonlinearity, which is mainly due to incomplete curvature correction and to the exponential increase of leakage currents at high temperatures.

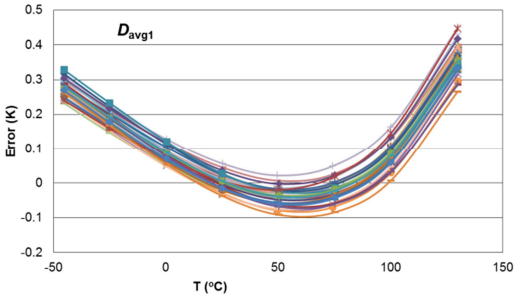

Fig. 10. Systematic error versus temperature for 36 samples when the duty cycle is calculated with Eq. 3 or 5 (D_{avg1} or D_{avg3}).

Fig. 11 shows the measured total error for the case that the average duty cycle is calculated with the simpler Eq. 4 (D_{avg2}). As expected, there is significantly more error at low temperatures. However, this error is still less than 0.1°C for the temperature range from 0°C to 110°C. Note that this is more than the simulated error shown in Fig. 7 and varies from sample to sample, depending on the specific combination of offset and component mismatch.

Taking into account the spread over different fabrication batches of wafers, the sensor's inaccuracy is specified as:

0.25°C for the temperature range of -10°C to 100°C
0.80°C for the temperature range of -45°C to 130°C

An even better accuracy can be achieved by accommodating the sensor's residual nonlinearity with a higher-order polynomial. Applying a least-squares-fit on the measurement results shown in Fig. 10, the relationship between duty cycle D and temperature ϑ, is found to satisfy the following third-order polynomial:

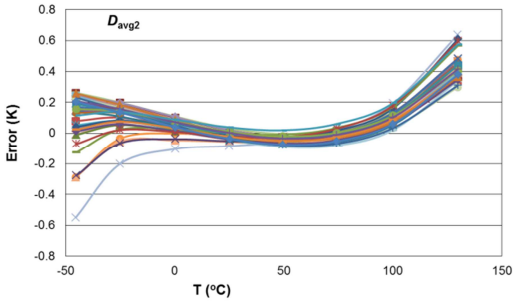

Fig. 11 Systematic error versus temperature for 36 samples, when the duty cycle is calculated with Eq. 4 (D_{avg2}).

$$D = a_0 + a_1\vartheta + a_2\vartheta^2 + a_3\vartheta^3 \qquad (6)$$

where $a_0 = 0.32$

$a_1 = 4.68 \times 10^{-3}$ / (°C)

$a_2 = 7.03 \times 10^{-8}$ / (°C)^2

$a_3 = 1.10 \times 10^{-9}$ / (°C)^3

ϑ = temperature in °C.

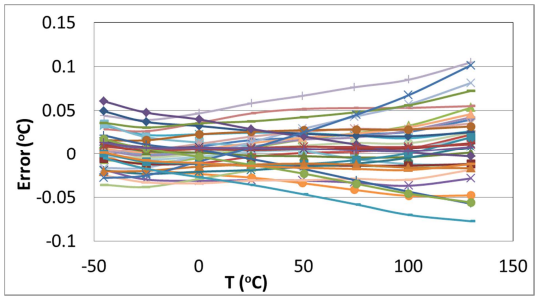

Fig. 12 Error versus temperature for 36 TO-18 samples (D_{avg1} and Eq. 6, V_{CC} =5V)

Fig. 12 shows the residual inaccuracy after computing D_{avg1} and applying Eq. 6, which is less than ±0.15°C from -45°C to 130°C.

The results presented so far reflect the performance of just one batch of sensors. To take batch-to-batch variation into account, the accuracy of the final product has been more conservatively specified:

0.10°C for the temperature range of -20°C to 70°C
0.30°C for the temperature range of -45°C to 130°C

A full list of specifications of the final product is presented in [22].

C. *Noise*

The sensor noise was determined by logging the results of 360000 measurements at a stable temperature (~25°C). A microcontroller with a 72MHz sampling frequency was used to digitize the time intervals. As shown in Fig. 13, the resolution amounts to about 3mK (rms) for the minimum measurement time t_m of 1.8ms (8 periods). The sensor's energy efficiency can be benchmarked with the help of the resolution Fig. of Merit (FoM) F, which is defined as follows [16]:

$$F = E \cdot s^2 \qquad (7)$$

where E is the energy consumed during one complete measurement (one DEM cycle) and s is the sensor's resolution (standard deviation). For a supply voltage of 3.3V, a supply current of 60µA, and a measurement time t_m of 1.8ms (8 periods), energy for one measurement E is only 356nJ. The sensor's resolution FoM is 3.2pJK^2, which is more than 100 times better than that of [1]. Averaging over 100ms improves the measurement resolution to 0.4mK (standard deviation), as shown in Fig. 13. Note that even for measurement times t_m up to 10s, the resolution continues to improve with $\sqrt{t_m}$ and becomes as low as 40 µK!

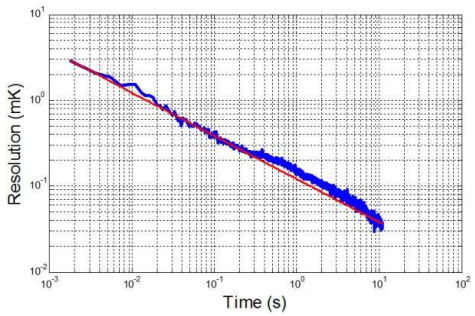

Fig. 13. Measured resolution versus measurement time (72MHz sampling frequency).

It should also be noticed that in a sensor system where a microprocessor is used to digitize the time intervals, the quantization noise due to the limited counter clock should be taken into account [17].

D. *Supply-voltage sensitivity*

Fig. 14 shows the change of the sensor's error (determined from D_{avg1}) versus supply voltage for three temperatures, referred to the errors at V_{CC} = 5V. Over the whole temperature range, the output varies by less than 0.1°C over the supply-voltage range from 2.7V to 5.5V.

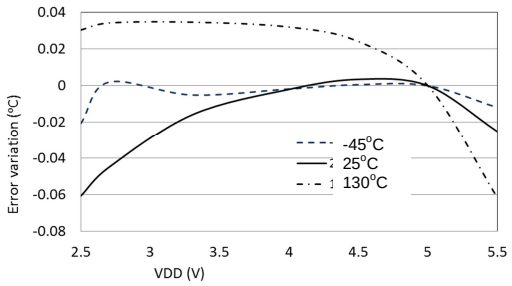

Fig. 14. Variation of sensor output with supply voltage, relative to its output with a 5V supply.

E. *Output driving capability*

The sensor's output buffer was designed to drive up to 20m long shielded cables. Fig. 15 shows measurement results from 5 samples for three different cable lengths. For supply voltages ranging from 3.3V to 5.5V, cable lengths up to 20m cause less than 50mK extra error over the whole temperature range -45°C to 130°C. For supply voltages lower than 3.3V, however, the sensor's output frequency increases and so the cable's capacitive load can cause significant errors.

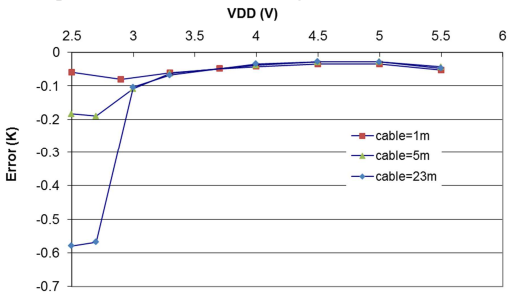

Fig. 15. Error versus supply voltage for different cable length at room temperature.

F. *Packaging and packaging shift*

To meet different market requirements, the new temperature sensor has been packaged in metal can (TO-18) as well as in low-cost plastic (TO92 and TO220). Due to differences in the thermal expansion coefficients of the various materials involved (silicon die, eutectic die attachment and metal substrate), some stress remains after the packaging process is finished and the device has cooled down to room temperature. Plastic packages induce much more stress than metal-can packages (i.e. TO-18) because they use an epoxy resin that completely covers the chip [10] [11]. Due to the piezo-junction effect, packaging-induced stress will cause the base-emitter voltage V_{BE3} (Fig. 4) to deviate from its nominal value and thus induce extra error in the sensor's output. As shown in [9] - [11], vertical PNPs are much less stress sensitive than the vertical NPNs used in [2], and so the new sensor should have less packaging shift and better stability.

Packaging shift has been investigated for the three different packages (TO-18, TO-92 and TO-220)., The average values of the temperature error at room temperature for each package are listed in Table 1. This table includes also the similar values for the previous BiCMOS design in TO-18 and TO-92 packages [1]. These values represents the packaging shift caused by package-induced mechanical stress.

Table 1 Packaging shift for three types of package compared with [1]

	TO-18 this design	TO-92[1] this design	TO-220[1] this design	TO-18 [1]	TO-92[1] [1]
number of sensors	36	18	9	18	18
Error (°C)	<10mK	0.044	0.053	-0.026	0.38
Spread (3σ) (°C)	0.06	0.13	0.06	0.31	0.35

[1]: The plastic packages employ a stress-relieving die coating.

The results in Table 1 show that, at room temperature, the error induced by the metal-can package (TO-18) is almost negligible. The plastic packages induce a positive shift, which is much smaller than that of the previous product. The difference between the TO-92 and TO-220 packages is very small. The larger spread of the TO-92 samples is probably due to the spread in package-induced stress, and holds for the whole temperature range. However, it is still much smaller than that of the TO-92 samples of [1]. These results represent a remarkable improvement on [1], and can be attributed mainly to the use of vertical PNPs rather than NPNs as sensing elements.

G. *Stability*

The sensor's stability has been tested in different ways:

a) *Hysteresis*: samples were cycled from 130°C to -45°C and then back to 130°C.
b) *Thermal shock*: samples were heated above 100°C and then rapidly cooled below 0°C.
c) *48-Hour test at high temperature:* samples were heated up to 200°C for 48 hours.
d) *Long-term stability*: samples were continuously operated for 72 days, and periodically tested at a stabilized temperature.

Measurement results on 14 samples (TO-18) shows that the hysteresis is less than 20mK (at 130°C). After thermal shocks, no measurable changes (<10mK) in the sensor's duty-cycle was observed. After being heated at 200°C for 48 hours,

only a rather small change (<50mK) has been found among 36 samples, which is probably caused by changes in the packaging-induced stress.

Long-term stability tests have been performed by a certification-qualified company (Tempcontrol I.E.P. B.V.). Eight sensors (never powered-on after wafer calibration) were inserted in a metal tube filled with thermal conductive paste. This tube was then put in a water bath, whose temperature was controlled to be at 22°C with an inaccuracy of 0.5mK. Over 72 days, as shown in Fig. 16, the sensor's output drift was found to be less than ±2.5mK.

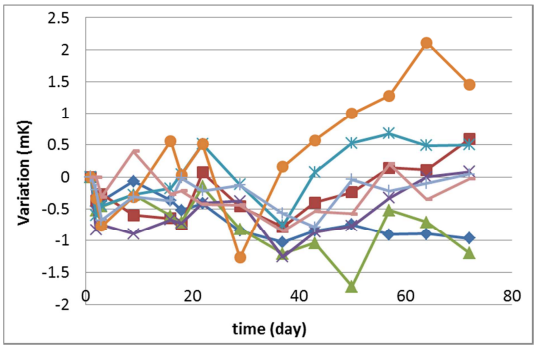

Fig. 16 Variation of temperature output over 72 days for 8 samples at 22°C.

H. Performance summary and comparison with other products

Table 2 summarizes the important features of this design compared to existing products in the market. It can be seen that this design achieves better accuracy and resolution, as well as higher speed.

Table 2 Comparison with other state-of-the-art temperature sensors.

	This design	SMT160 [1]	D18B20 [18]	LM73 [19]	TMP102 [20]	ADT7320 [21]
Supply voltage (V)	2.7 to 5.5	4.75 to 7.2	3.0 to 5.5	2.7 to 5.5	1.4 to 3.6	2.7 to 5.5
Supply current (µA)	42 to 75	180	1000 to 1500 (at 5V)	250 to 495 (at 5V)	10 to 85	210 to 300
Number of pins	3 or 4	3	3	6	6	12
Temperature range (°C)	-45 to 130	-45 to 130	-55 to 125	-40 to 150	-40 to 125	-40 to 125
Output signal	DCM	DCM	digital	digital	digital	digital
Measurement time (ms)	1 to 22	0.25 to 2	94 to 750	10 to 112	26 to 35	240
Supply voltage Sensitivity (°C/V)	0.1	0.1	0.1	-	0.2	0.1
Best Accuracy (°C) Temperature range (°C)	0.1[1] (-20 to 70)	0.7 (-10 to 100)	0.5 (-10 to 85)	1.0 (-10 to 80)	0.5 (-25 to 85)	0.5 (-10 to 105)
	0.3[1] (-45 to 130)	1.2 (-45 to 130)	2 (-55 to 125)	2.5 (-40 to 150)	3 (-55 to 125)	0.66 (-40 to 125)
Resolution (°C) Measurement time (ms)	0.003 1.8	0.005 20	0.0625 750	0.03125 112	0.0625 250	0.0078 240
Resolution FoM (pJK^2)	3.2	430	1.46×10^7	1.37×10^5	1.37×10^4	8.28×10^3

[1]: The accuracy in this table is the result using Eq. 6 and D_{avg1}/D_{avg3}.

It should be noticed that the above mentioned resolution FoM doesn't include the energy needed for digitizing the time intervals of the sensor output. This is also the reason why this value is much lower than that of some products listed in Table 2, which have digital outputs. Yet the low Resolution FoM enables this sensor to be used in a low-power system, for instance battery-powered and/or wireless sensor systems.

VII. CONCLUSIONS

A CMOS BJT-based temperature sensor has been designed and fabricated. Its duty-cycle-modulated output enables easy interfacing with both the digital and the analog domains, making it well suited to temperature monitoring and controlling. Applying DEM and chopping significantly reduces the systematic errors caused by CMOS component mismatch. Applying substrate PNP instead of NPN transistors reduces error caused by package-induced stress. Low-cost wafer-level trimming at room temperature reduces the error due to process spread. As a result, better accuracy has been achieved compared to the predecessor. Three methods of computing the sensor's output duty-cycle have been presented. These methods provide different trade-offs between computational speed/complexity and sensing accuracy.

Measurement results show that this temperature sensor achieves an excellent resolution Figure of Merit: better than (3.2pJK^2), which makes this sensor highly suited for low-energy applications. After wafer calibration at room temperature, the sensor's accuracy is better than 0.1°C (-20°C to 70°C) and 0.3°C (-45°C to 130°C), respectively. Package-induced errors were found to be less than 0.1°C at room temperature.

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