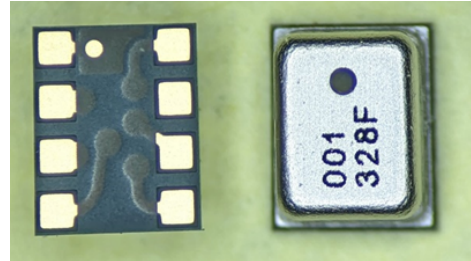


## **PBM210-A20K series**

### **Digital pressure sensor**

#### **Features**

- Supply voltage:
  - 1.7 to 5.5V(V<sub>DD</sub>)
  - 1.2 to 5.5V(V<sub>DDIO</sub>)
- Absolute pressure range 30 to 200 kPa
- 2.2ms fastest conversion time
- Standby current <0.1μA
- I<sup>2</sup>C and SPI interfaces
- Calibrated and temperature compensated



#### **Application Examples**

- Indoor and outdoor navigation
- Weather forecast device
- Altimeter and barometer for portable device
- Bike computer

#### **Descriptions**

The PBM210 is a new generation of high resolution digital barometer. The PBM210 is a digital pressure sensor which consists of a MEMS piezoresistive pressure sensor and a signal conditioning ASIC. The ASIC include a 24bits sigma-delta ADC, OTP memory for calibration data, and serial interface circuits. The PBM210 could provide both I<sup>2</sup>C and SPI interface to communicate with microcontroller.

Pressure calibrated and temperature compensated were key features of the PBM210. The data stored in OTP memory could be used to calibrate the PBM210. The calibration procedure should be implemented by a external microprocessor. The PBM210 is low power and supply voltage designed and suitable for portable devices or battery-supplied ones.

#### **Ordering information**

Part No.	Pressure type	Pressure range	Digital interface	Package	Note
PBM210-A20KDR	Absolute	30-200kPa	SPI / I <sup>2</sup> C	LGA	Tape & Reel

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## 1 Functional Block and Pin Descriptions

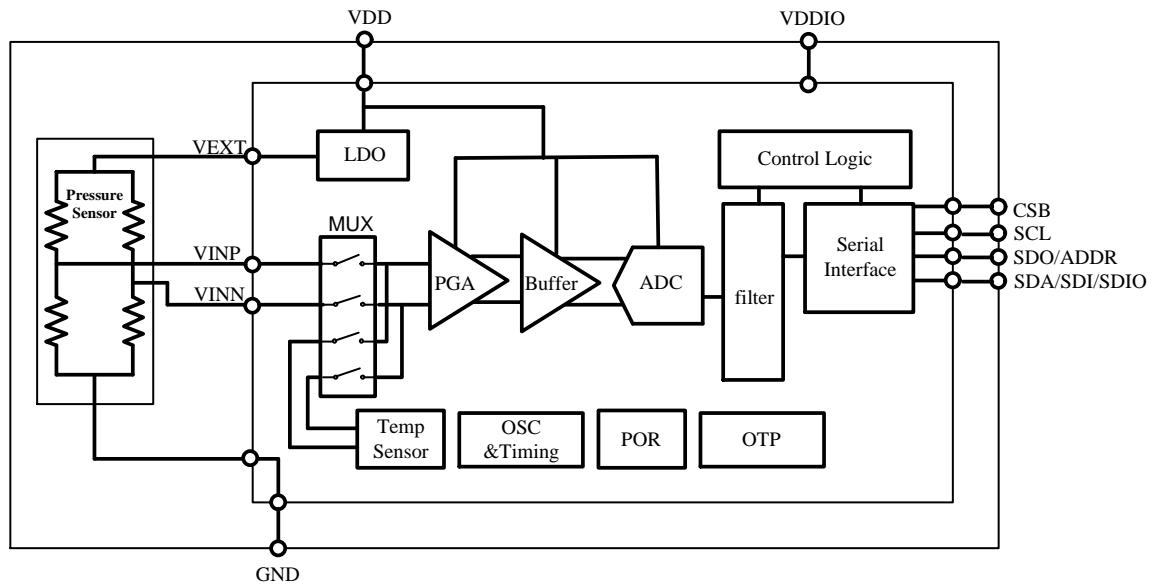
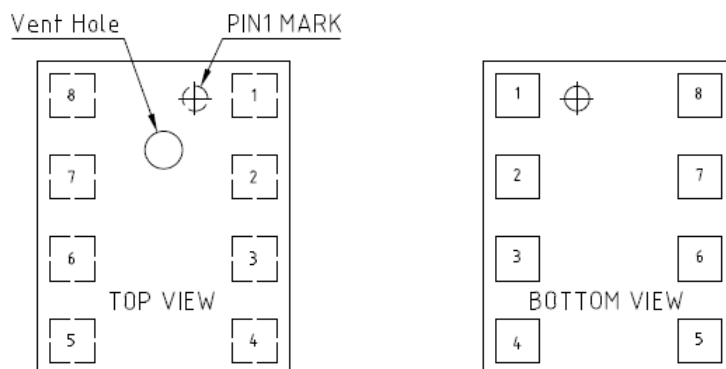


Fig. 1 Functional Block Diagram of PBM210



Pin No.	Pin Name	Description
1	GND	Ground
2	CSB	Chip Select
3	SDA/SDI/SDIO	Serial data input/output in I <sup>2</sup> C mode(SDA) Serial data input in 4-wire SPI mode(SDI) Serial data input/output in 3-wire SPI mode (SDIO)
4	SCL	Serial clock
5	SDO/ADDR	Serial data output in 4-wire SPI mode Address select in I <sup>2</sup> C mode
6	V <sub>DDIO</sub>	Power supply for I/O circuits
7	GND	Ground
8	V <sub>DD</sub>	Power supply for core circuits

## 2 Electrical Characteristic

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Pressure Range			30		200	kPa	
Operating Temperature Range			-40		85	°C	
Supply Voltage	V <sub>DD</sub>		1.7	1.8	5.5	V	
	V <sub>DDIO</sub>		1.2	1.8	5.5	V	
Supply Current							
Pressure measurement	I <sub>DD</sub>	1 conversion/sec.					
Ultra low power				3.0	3.5		
Standard				4.7	6.4		μA
High resolution				7.7	8.9		
Ultra high resolution				13.9	16.0		
Temperature measurement			1.9	2.2			
Peak Current During Conversion							
Pressure measurement	I <sub>peak</sub>			1.51		mA	
Temperature measurement				0.95			
Standby Current	I <sub>sd</sub>			<0.1		μA	
Conversion time							
Pressure measurement							
Ultra low power				2.2	2.5		
Standard				3.3	3.7	ms	
High resolution				5.4	6.0		
Ultra high resolution				9.8	10.7		
Temperature measurement				2.2	2.5		
Offset temperature coefficient		90 kPa 25~40°C		3	5	Pa/K	
Absolute Pressure Accuracy V <sub>DD</sub> =3.3V		30~200 kPa -20~0°C		±4	±6	hPa	3
		30~200 kPa 0~65°C		±2	±3	hPa	
Resolution in ultra high resolution mode		Pressure Temperature		0.02 0.01		hPa °C	4
Noise in pressure							
Ultra low power				3.94			RMS noise
Standard				2.92		Pa	
High resolution				2.32			
Ultra high resolution				1.96			
Absolute temperature accuracy V <sub>DD</sub> =3.3V		@25°C 0~65°C	-1.5 -2	±0.5 ±1	1.5 2	°C	
Soldering drift		After solder reflow	-0.2		0.2	kPa	
Long term stability		12 months	-0.1		0.1	kPa	
1. All the data were measured with 1.8V supply voltage at a temperature of 25±3°C, unless otherwise noted. 2. Maximum error of pressure reading over the pressure range after offset adjusted at one pressure point. 3. Maximum error of pressure reading over the pressure range. 4. According to 32 bit integer compensation formula.							

## 3 Absolute Maximum Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	AVDD		-0.3		6.5	V	
	VDDIO		-0.3		6.5	V	
Digital output voltage			-0.3		VDDIO+ 0.3	V	

Storage Temperature Range			-40		125	°C	
Maximum Overpressure					10	bar	
ESD Rating							
HBM				2		kV	

### 4 Application Information

Owing to state of the art, the PBM210 build a new standard of digital barometer. A 24bits sigma-delta ADC and a MEMS pressure sensor are integrated in a LGA substrate. Pressure calibrated and temperature compensated were key features of the PBM210. The PBM210 is low power and supply voltage designed and suitable for portable devices or battery-supplied ones.

The data stored in OTP memory could be used to calibrate the PBM210. The calibration procedure should be implemented by an external microprocessor. By I<sup>2</sup>C or SPI interface, you can get the calibration data stored in OTP and the raw data of pressure and temperature. In order to get the correct pressure and temperature reading, the calculating procedure must be implemented in a microprocessor.

#### Application Circuit example

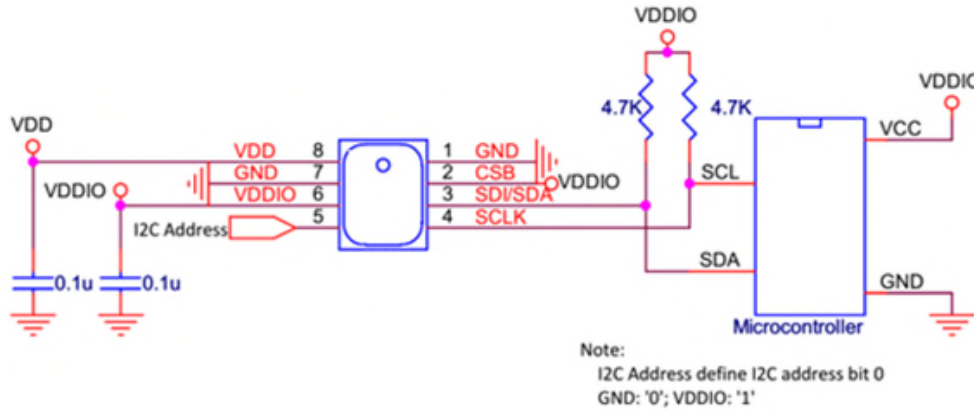


Figure. 4.1 Application circuit for I<sup>2</sup>C interface

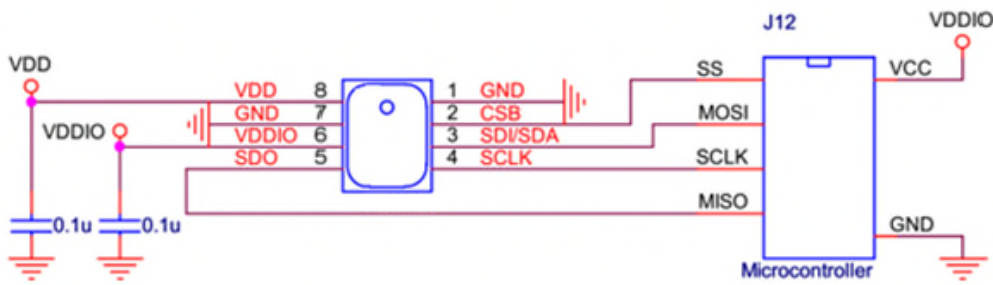


Figure 4.2 Application circuit for SPI interface

## 5 Control registers

Table 5.1 control registers

Addr	Description	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0xF8	DATA_LSB	R	Data out<7:0>								0x00
0xF7	DATA_CSB	R	Data out<15:8>								0x00
0xF6	DATA_MSB	R	Data out<23:16>								0x00
0xF4	CONFIG_1	RW	OSR<1:0>		Measurement_control<5:0>					0x0E or 0x4E	
0xF1	Cal_coeff	R	Calibration Registers								N/A
0xE0	Soft_reset	W	Softreset<7:0>								0x00
0xD0	Cal_coeff	R	Calibration Registers								N/A
0xBB-0xAA	Cal_coeff	R	Calibration Registers								N/A
0x6B	Part ID	R	PartID<7:0>								0x42
0x00	SPI_Ctrl	RW	SDO_active	LSB_first					LSB_first	SDO_active	0x00

### Reg 0xF6–0xF8

**Data\_out:** 24 bits ADC output data

### Reg 0xF4

**OSR<1:0>:** 00:1024X, 01:2048X, 10:4096X, 11:8192X

**Measurement\_control<5:0>:** 101110, indicate a temperature conversion. 110100, indicate a pressure conversion.

### Reg 0xE0

**Softreset :** Write only register. If set to 0xB6, will perform a power on reset sequence. Auto returned to 0 after the soft reset completed.

### Reg {0xF1, 0xD0, 0xBB:0xAA}

**Calibration Registers :** Total 20bytes calibration registers used for sensor calibration.

### Reg 0x6B

**PartID:** 8 bits Part ID, the default value is 0x42.

### Reg 0x00

**SDO\_active:** 1: 4-wire SPI, 0: 3-wire SPI

**LSB\_first:** 1: LSB first for SPI interface, 0: MSB first for SPI interface

Table 5.2 Summary of instructions

Instruction	Register address	Value
-------------	------------------	-------

Pressure measurement, OSR1024	0xF4	0x34
Pressure measurement, OSR2048	0xF4	0x74
Pressure measurement, OSR4096	0xF4	0xB4
Pressure measurement, OSR8192	0xF4	0xF4
Temperature measurement	0xF4	0x2E
Softreset	0xE0	0xB6
3-wire SPI, MSB first	0x00	0x00
4-wire SPI, MSB first	0x00	0x81

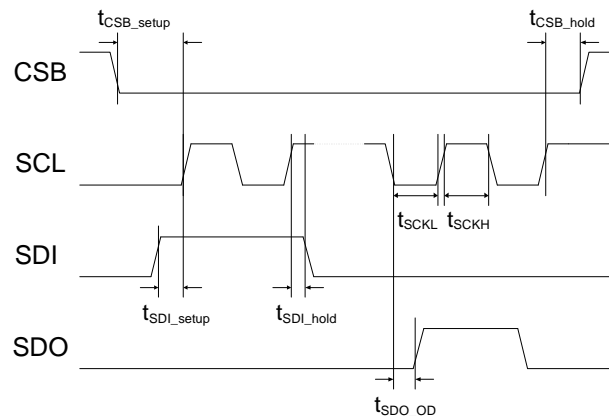
## 6 SPI Interface

PBM210 provides both SPI and I<sup>2</sup>C interface for serial communication and 'CSB' pin is used to switch between these two protocols. Pulling 'CSB' pin low selects the SPI interface, leaving 'CSB' pin float or pulling it high selects the I<sup>2</sup>C interface. The SPI interface is compatible with SPI mode 0 (CPOL=0, CPHA=0).

Table 6.1 SPI interface specifications

Symbol	Parameter	Condition	Min	Max	Unit
$f_{\text{sclk}}$	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
$t_{\text{sclk}_l}$	SCLK low pulse		20		ns
$t_{\text{sclk}_h}$	SCLK high pulse		20		ns
$T_{\text{sdi\_setup}}$	SDI setup time		20		ns
$T_{\text{sdi\_hold}}$	SDI hold time		20		ns
$T_{\text{sdo\_od}}$	SDO/SDI output delay	Load = 25pF		30	ns
		Load = 250pF		40	ns
$T_{\text{csb\_setup}}$	CSB setup time		20		ns
$T_{\text{csb\_hold}}$	CSB hold time		40		ns

The figure below shows the definition of the SPI timing given in table 6.1



### Figure 6.1 SPI timing diagram

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in Figure 6.2, the instruction phase is divided into a number of bit fields.

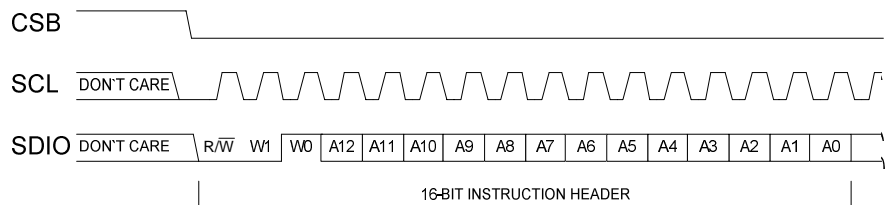


Figure 6.2 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read is being requested, otherwise indicates it is a write operation.

W1 and W0 represent the number of data bytes to transfer for either read or write (Table 6.2). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a nonbyte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table 6.2 W1 and W0 settings

W1:W0	Action	CSB stalling
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional
11	4 or more bytes of data can be transferred. CSB must be held low for entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). This can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB\_first' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed. (Figure 6.3)



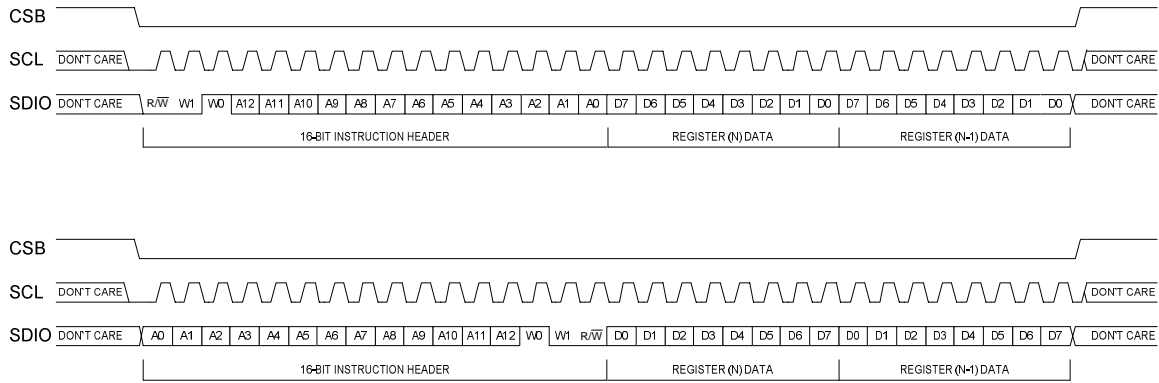


Figure 6.3 MSB First and LSB First Instruction and Data Phases

Register bit 'SDO\_active' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDIO pin. If this bit is set, read data is placed on the SDO pin. The instruction and data phase is as shown in figure 6.4. The default for this bit is low, making SDO inactive.

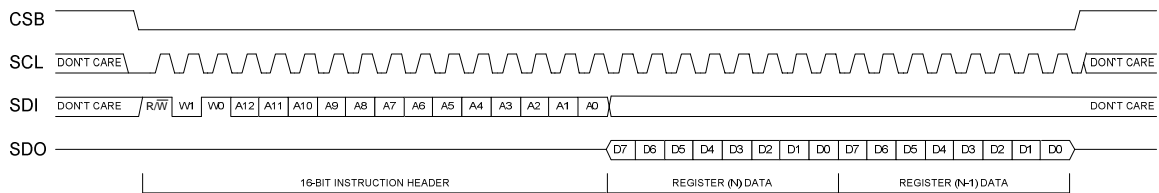


Figure 6.4 MSB First Instruction and Data Phases for 4-wires SPI Mode

## 7 I<sup>2</sup>C Interface

I<sup>2</sup>C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I<sup>2</sup>C device address of PBM210 is shown below. The LSB bit of the 7bits device address is configured via SDO/ADDR pin. If the SDO/ADDR pin was left not connected or pulled high, the A1 bit is "1". And the device address is "1101101". For I<sup>2</sup>C bus application, 'CSB' pin have to be left float or pulled high.

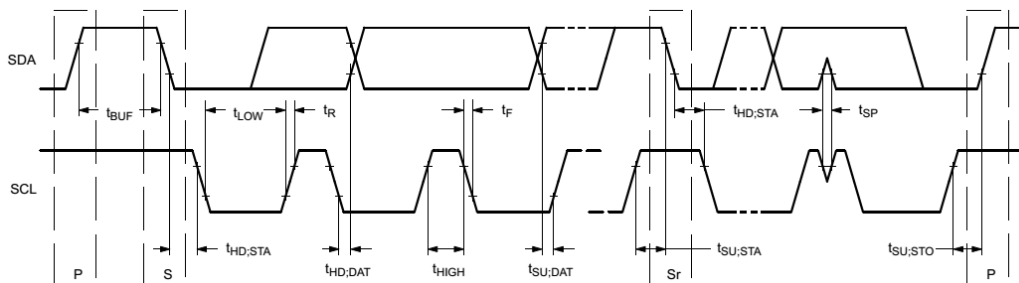
Table 7.1 I<sup>2</sup>C Address.

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	0	1	1	0	SDO/ADDR	0/1

Table 7.2 Electrical specification of the I<sup>2</sup>C interface pins

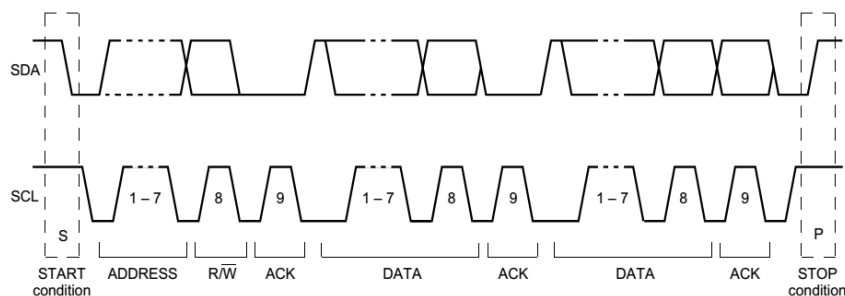
Symbol	Parameter	Condition	Min	Max	Unit
f <sub>scl</sub>	Clock frequency			400	kHz
t <sub>LOW</sub>	SCL low pulse		1.3		us
t <sub>HIGH</sub>	SCL high pulse		0.6		us

$t_{SUDAT}$	SDA setup time		0.1		us
$t_{HDDAT}$	SDA hold time		0.0		us
$t_{SUSTA}$	Setup Time for a repeated start condition		0.6		us
$t_{HDSTA}$	Hold time for a start condition		0.6		us
$t_{SUSTO}$	Setup Time for a stop condition		0.6		us
$t_{BUF}$	Time before a new transmission can start		1.3		us

Figure 7.1 I<sup>2</sup>C Timing Diagram

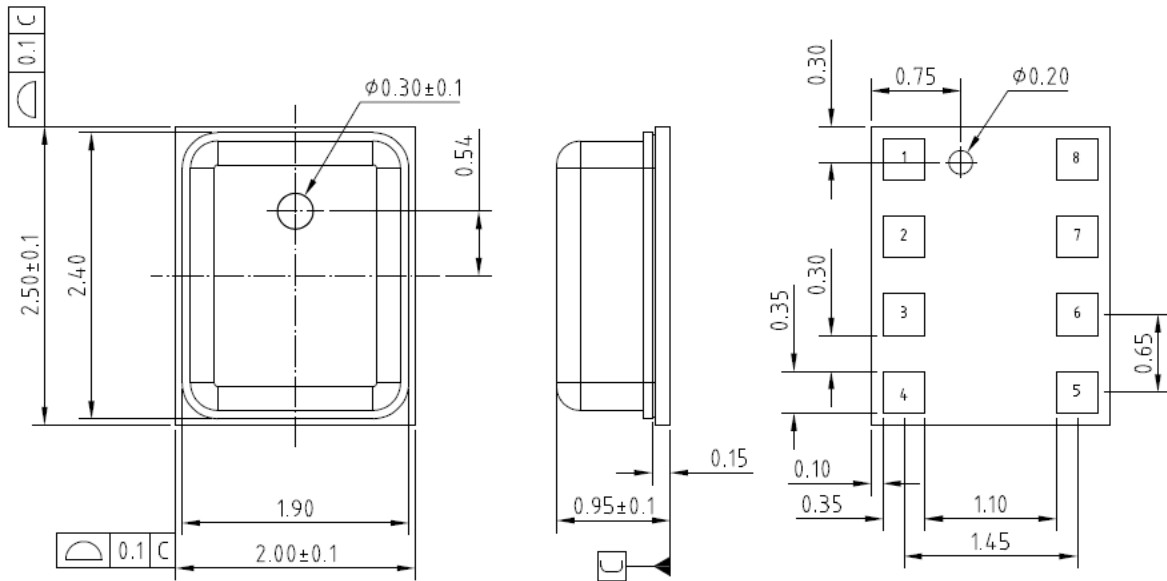
The I<sup>2</sup>C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

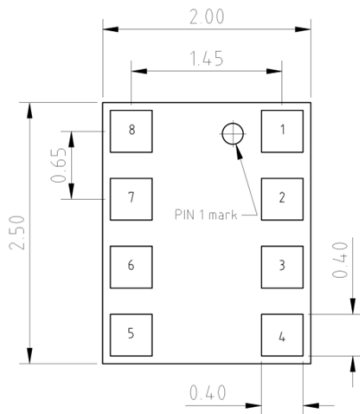
Figure 7.2 I<sup>2</sup>C Protocol

## 8 Package Information

### 8.1 Outline dimensions



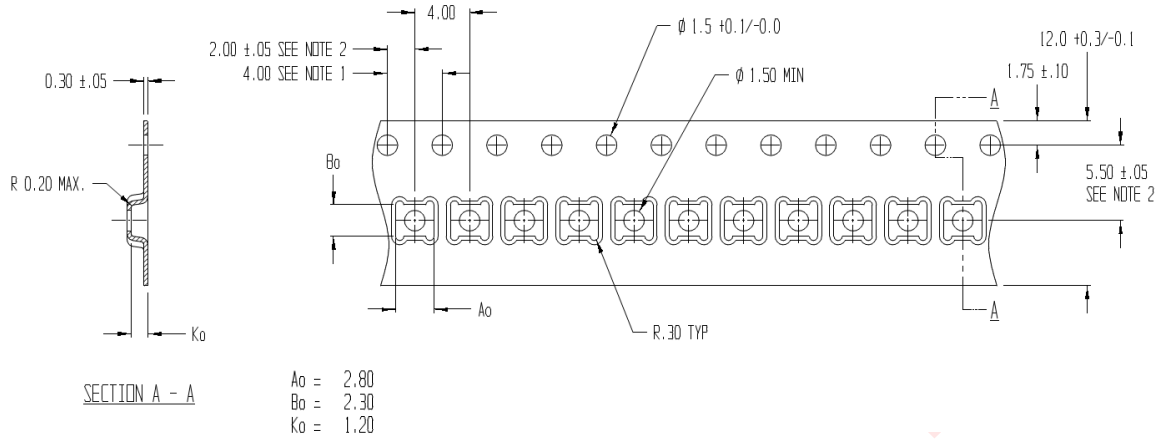
### 8.2 Recommended footprint



All dimensions are in mm.

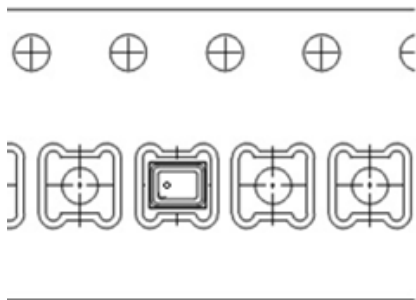
### 8.3 Tape and Reel specification

#### 8.3.1 Tape dimensions



All dimensions are in mm.

#### 8.3.2 Sensor orientation relative to the tape



## 9 Document history and modification

Rev.	Description	Date
1.0	First edition (Formal release)	2016/01/21
1.1	2. Electrical characteristic, kpa->hPa, page 4	2017/02/14
1.2	Resolution in ultra high resolution mode, Pressure, 0.02 hpa, page 4	2022/01/27
1.3	Modified: Product outline, page 1, 3, 11	2024/01/30

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