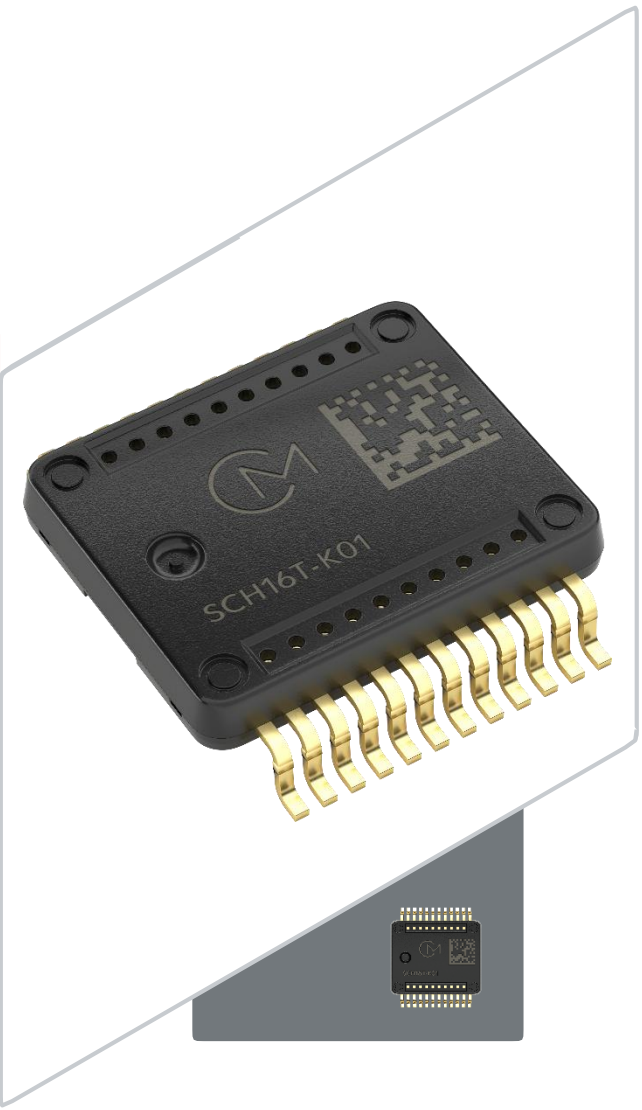
SCH16T-K01 Data Sheet

6-DOF XYZ-Axis gyroscope and XYZ-Axis accelerometer with digital SPI interface



Features

- ±300 °/s calibrated angular rate measurement range.
- ±80 m/s² calibrated acceleration measurement range
- Auxiliary digital accelerometer channel with up to ±260 m/s² dynamic range
- Options for output interpolation and decimation
- Angular rate and acceleration low pass filters from 13Hz to 370 Hz cut-off rate
- Data Ready output, timestamp index and SYNC input functions for clock domain synchronization.
- -40...110 °C operating temperature range
- 3.0...3.6 V supply voltage, 1.7…3.6 V I/O supply voltage
- SafeSPI v2.0 interface
- 20-bit and 16-bit output data, selectable via SPI frame
- Extensive self-diagnostic features
- 11.8 mm x 13.4 mm x 2.9 mm (l x w x h) SOIC-24
- Qualification based on AEC-Q100 standard

Applications

SCH16T series is targeted at applications demanding high performance with tough environmental requirements. Typical applications include:

- Inertial measurement units (IMUs)
- Inertial navigation and positioning
- Machine control and guidance
- Dynamic inclination
- Robotic control and UAVs

Application restriction

- https://www.murata.com/en-global/support/militaryrestriction

Overview

The SCH16T is a combined high-performance 3-axis angular rate and 3-axis accelerometer. The angular rate and accelerometer sensor elements are based on Murata's proven capacitive 3D-MEMS technology. Signal processing is done by a single mixed-signal ASIC that provides angular rate and acceleration via a flexible SafeSPI v2.0 compliant digital interface. Sensor elements and ASIC are packaged to pre-molded SOIC 24-pin plastic housing that guarantees reliable operation over the product's lifetime.

The SCH16T is designed, manufactured, and tested for high stability, reliability, and quality requirements. The component has extremely stable output over temperature, humidity, and vibration. The component has several advanced self-diagnostic features, is suitable for SMD mounting and is compatible with RoHS and ELV directives.

TABLE OF CONTENTS

1 Introduction

This document contains essential technical information about the SCH16T sensor including specifications, SPI interface descriptions, user-accessible register details, electrical properties, and application information. This document should be used as a reference when designing in the SCH16T component.

2 Product types and order codes with packing quantity

Table 1 Product types and order codes

Product Type	Description	Packing	Quantity
SCH16T-K01-004	Gyroscope ±300 dps, Accelerometer ±80 m/s²	Sample package, Bulk	4 pcs
SCH16T-K01-1		Tape & Reel	100 pcs
SCH16T-K01-10		Tape & Reel	1000 pcs

3 Specifications

3.1 Abbreviations

ACC	Accelerometer
ARS	Angular Rate Sensor (gyroscope)
ASIC	Application Specific Integrated Circuit
CS	Chip Select
DPS	Degrees Per Second
DRY	Data Ready
F_PRIM	Gyroscope Primary Frequency
FREQ	Frequency
Gyro	Gyroscope
LPM	Low Power Mode
LPF	Low-Pass Filter
MCU	Microcontroller Unit
MEMS	Micro-Electro-Mechanical System
MISO	Master In Slave Out
MOSI	Master Out Slave In
PD	Pull Down
PU	Pull Up
RT	Room Temperature
SCK	Serial Clock
SPI	Serial Peripheral Interface
SYNC	Synchronization

3.2 General specifications

Table 2 General specifications for SCH16T series

Parameter	Min	Nom	Max	Unit
Operating Temperature	-40		110	°C
Supply Voltage	3.0	3.3	3.6	V
Digital I/O supply	1.7		3.6	V
Total Supply Current	36	41	47	mA
Low Power Mode current consumption			10	mA
Gyro Primary Frequency, F_PRIM	22.1	23.6	25.1	kHz
Output update rate - Interpolated outputs (F_PRIM x 16)	353.6	377.6	401.6	kHz
Output update rate - Decimated outputs		23.6/X (1		kHz
Turn-on-time (2			250	ms

1) Decimation ratio X is selectable from the following options: 2, 4, 8, 16 and 32
2) After voltage supplies are within specification

3.3 Absolute maximum ratings

Murata guarantees sensor operation without parameter related damage or functional deviation within these maximum ratings. However, output values may deviate from specification if parameter values are outside limits defined in *Performance specifications for gyroscope* and *Performance specifications for accelerometer*. All voltages are related to the potential at GND.

Table 3 Absolute maximum ratings

Parameter	Remark	Min	Nom	Max	Unit
Supply voltage	Supply voltage (pins V3P3, VDDIO)	-0.3		3.63	V
Voltage at Analog input/output pins		-0.3		3.63	V
Voltage at Digital input/output pins		-0.3		3.63	V
Storage Temperature	Within these maximum ratings no damage to the component shall occur in an instant or up to max 24 hours	-50		150	°C
ESD_HBM	ESD according to Human Body Model (HBM), Q100-002	2000			V
ESD_CDM center pins	Center pins ESD according to Charged Device Model (CDM), Q100-011	500			V
ESD_CDM corner pins	corner pins ESD according to Charged Device Model (CDM), Q100-011	750			V
Ultrasonic agitation	Cleaning, welding, etc.		Prohibited		

3.4 Performance specifications for gyroscope

Table 4 Performance specifications for all measurement axes, supply voltage = 3.3 V and at room temperature unless otherwise specified

Parameter	Condition	Min (-3 σ)	Nom	Max (+3 σ)	Unit
Measurement range [A]	Guaranteed valid specification range, lowest selectable sensitivity setting	±300			°/s
	Guaranteed valid specification range, highest selectable sensitivity setting	±62.5			°/s
Offset [B]	-40 °C ... +110 °C	-0.6		0.6	°/s
Offset drift over temperature [C]	-40 °C ... +110 °C	-0.2		0.2	°/s
Offset drift over lifetime [D]	After HTOL 1000h	-0.2		0.2	°/s
Default sensitivity – 16-bit mode [E]			100		LSB/(°/s)
Default sensitivity – 20-bit mode [E]			1600		LSB/(°/s)
Sensitivity drift over temperature [F]	XY axis, -40 °C ... +110 °C	-0.3		0.3	%
	Z axis, -40 °C ... +110 °C	-0.2		0.2	%
Sensitivity drift over lifetime [G]	After HTOL 1000h	-0.3		0.3	%
Linearity error ±300 °/s [H]	-40 °C ... +110 °C		0.02	0.08	°/s
Noise density			0.0006		(°/s)/√Hz
Angle random walk [I]			0.015		°/√h
Bias instability [J]	Allan variance minimum divided by 0.664		0.5		°/h
Orthogonality error (between rate axes) [K]	-40 °C ... +110 °C	-0.15		0.15	%
G-sensitivity [L]	For DC gravity input			0.006	(°/s)/(m/s^2)

Notes:
• Specified Min/Max values contain ±3 sigma variation limits of original test population. Typical values are validation population mean (unless otherwise specified). Min/Max and typical values are not guaranteed, values represent validation population characteristics.
• Specification is valid after 24 hours from reflow.
• Each system design including SCH16T series component must be evaluated by the customer in advance to guarantee proper functionality during operation.

Table 5 Gyroscope parameter definitions

Symbol	Description
A)	Measurement range is tied to electrical headroom and is selectable from predefined options presented in *7.4.2*. Changing electrical headroom affects only signal path sensitivity (up to 4*nominal sensitivity).
B)	Initial offset at Murata production measurement after calibration
C)	Offset drift over temperature is determined by ((maximum offset value over temperature) - (minimum offset value over temperature)) / 2 in condition of one temperature sweep in specified temperature range.
D)	Estimated from offset drift during 1000 hours of high temperature operating life (HTOL) test at 125 °C and maximum supply voltages.
E)	Default sensitivity used in factory calibration. With this default sensitivity, signal has a typical electrical headroom of ±327.5 °/s.
F)	$Sensitivity = \frac{AR_{meas}(\Omega_{max}) - AR_{meas}(\Omega_{min})}{\Omega_{max} - \Omega_{min}}$ Where: Ω_{max} = applied angular rate at maximum operating range Ω_{min} = applied angular rate at minimum operating range $AR_{meas}(\Omega_n)$ = measured angular rate at Ω_n [LSB] Sensitivity drift over temperature is determined by [(maximum sensitivity value over temperature) - (minimum sensitivity value over temperature)] / 2 *100%
G)	Estimated from sensitivity drift during 1000 hours of high temperature operating life (HTOL) test at 125 °C and maximum supply voltages.
H)	Linearity error is the residual error remaining after a least-squares linear fit over measurement range. (Best fit linear model)
I)	Angle random walk is the white noise term estimated from Allan deviation at tau = 1s
J)	Allan variance minimum divided by 0.664. Optimization for SPI duty cycle or sample rate is required to achieve typical Allan variance in table. Device is powered on for four hours before data collection starts to permit full thermal stabilization.
K)	Rate axes are orthogonal if their intersecting angle is exactly 90°. Orthogonality error is the deviation from 90°.
L)	Angular rate offset sensitivity in respect to orientation in the earth gravitation. Contains 0.004 °/s from Earth's rotation. Can not be extrapolated beyond gravitation.

3.5 Performance specifications for accelerometer

Table 6 Performance specifications for all measurement axes, up to ±80 m/s² measurement range, supply voltage = 3.3 V and at room temperature unless otherwise specified

Parameter	Condition	Min (-3 σ)	Nom	Max (+3 σ)	Unit
Measurement range [A]	Guaranteed valid specification range, lowest selectable sensitivity setting	±80			m/s^2
	Guaranteed valid specification range, highest selectable sensitivity setting	±15			m/s^2
Offset [B]	-40 °C ... +110 °C	-0.14		0.14	m/s^2
Offset drift over temperature [C]	-40 °C ... +110 °C	-0.07		0.07	m/s^2
Offset drift over lifetime [D]	After HTOL 1000h	-0.05		0.05	m/s^2
Default sensitivity – 16-bit mode [E]			200		$LSB/(m/s^2)$
Default sensitivity – 20-bit mode [E]			3200		$LSB/(m/s^2)$
Sensitivity drift over temperature [F]	-40 °C ... +110 °C	-0.15		0.15	%
Sensitivity drift over lifetime [G]	After HTOL 1000h	-0.1		0.1	%
Linearity error [H]	Full Scale -40 °C ... +110 °C		0.06	0.15	m/s^2
	-1g…1 g, -40 °C ... +110 °C			0.01	m/s^2
Noise density			0.8		$(mm/s^2)/\sqrt{Hz}$
Velocity random walk [I]			30		$(mm/s)/\sqrt{h}$
Bias instability [J]	Allan variance minimum divided by 0.664		0.20		mm/s^2
Orthogonality error (between ACC axes) [K]	-40 °C ... +110 °C	-0.15		0.15	%

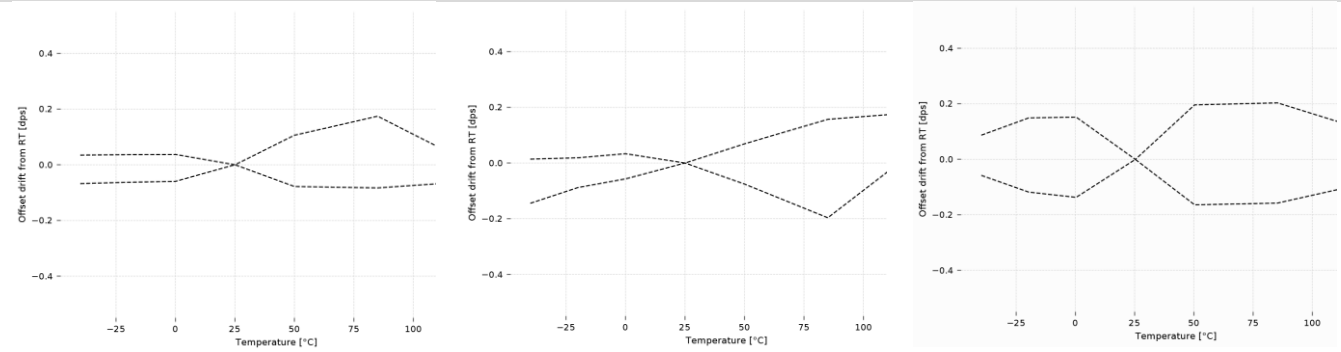
Notes:
• Specified Min/Max values contain ±3 sigma variation limits of original test population. Typical values are validation population mean (unless otherwise specified). Min/Max and typical values are not guaranteed, values represent validation population characteristics.
• Specification is valid after 24 hours from reflow.
• Each system design including SCH16T series component must be evaluated by the customer in advance to guarantee proper functionality during operation.
• A factor of 98 can be used when converting m/s^2 to milli-g. Actual gravity depends on sensor location on Earth.

Table 7 Accelerometer parameter definitions

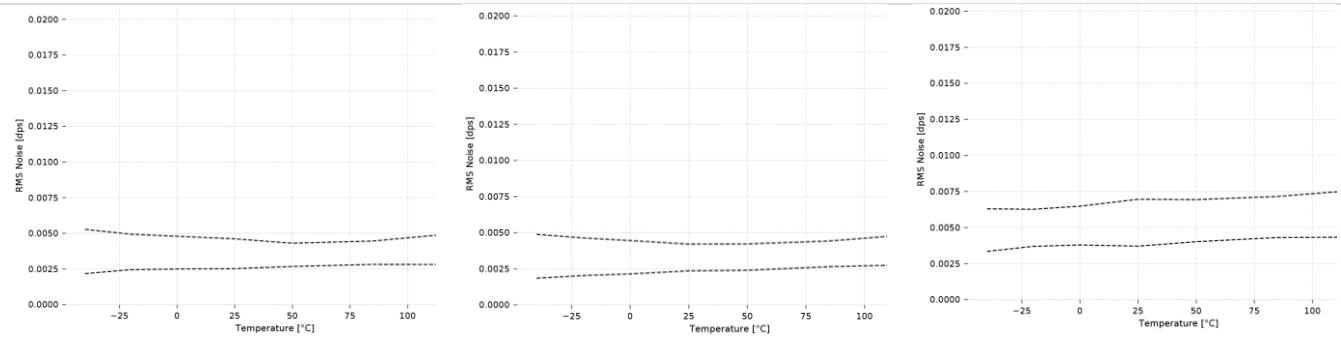
Symbol	Description
A)	Measurement range is tied to electrical headroom and is selectable from predefined options presented in *7.4.2*. Changing electrical headroom affects only signal path sensitivity (up to 4*nominal sensitivity).
B)	Initial offset at Murata production measurement after calibration
C)	Offset drift over temperature is determined by ((maximum offset over temperature) - (minimum offset over temperature)) / 2 in condition of one temperature sweep in specified temperature range.
D)	Estimated from offset drift during 1000 hours of high temperature operating life (HTOL) test at 125 °C and maximum supply voltages.
E)	Default sensitivity used in factory calibration. With this default sensitivity, signal has a typical electrical headroom of ±163.4 m/s^2.
F)	$Sensitivity = \frac{ACC_{meas}(a_{+1g}) - ACC_{meas}(a_{-1g})}{a_{+1g} - a_{-1g}}$ Where: a_{+1g} = applied acceleration at +1g (i.e., +1g gravity of manufacturing location) a_{-1g} = applied acceleration at -1g (i.e., -1g gravity of manufacturing location) $ACC_{meas}(a_n)$ = measured acceleration at a_n [LSB] Sensitivity drift over temperature is determined by [(maximum sensitivity value over temperature) - (minimum sensitivity value over temperature)] / 2 *100%
G)	Estimated from sensitivity drift during 1000 hours of high temperature operating life (HTOL) test at 125 °C and maximum supply voltages.
H)	Linearity error is the residual error remaining after a least-squares linear fit over measurement range. (Best fit linear model)
I)	Velocity random walk is the white noise term estimated from Allan deviation at tau = 1s
J)	Allan variance minimum divided by 0.664. Optimization for SPI duty cycle or sample rate is required to achieve typical Allan variance in table. Device powered on for four hours before data collection starts to permit full thermal stabilization.
K)	ACC axes are orthogonal if their intersecting angle is exactly 90°. Orthogonality error is the deviation from 90°.

3.6 Gyroscope typical performance characteristics

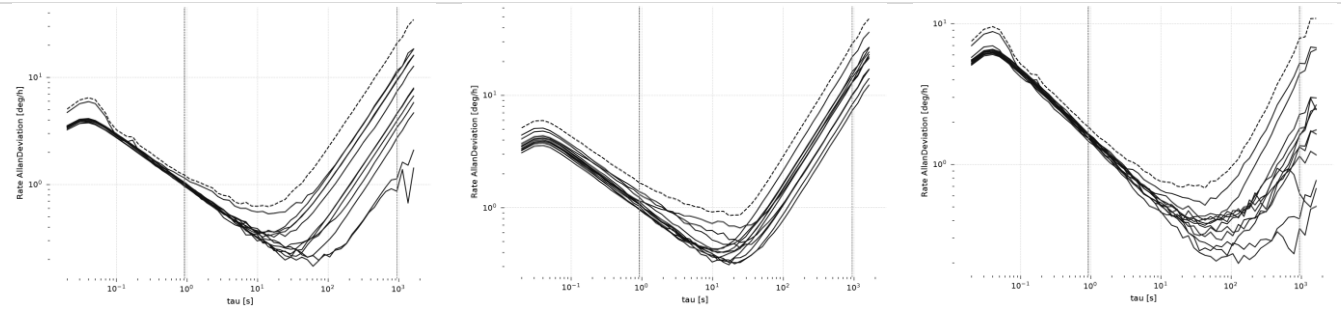
X-Axis	Y-Axis	Z-Axis



Offset drift over temperature from room temperature (°/s) 4 σ population limits



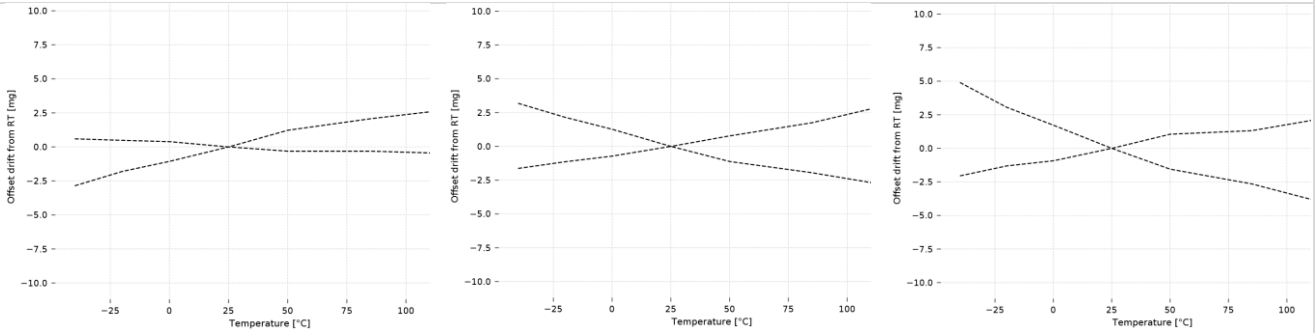
RMS noise 68 Hz LPF (°/sRMS) 4 σ population limits



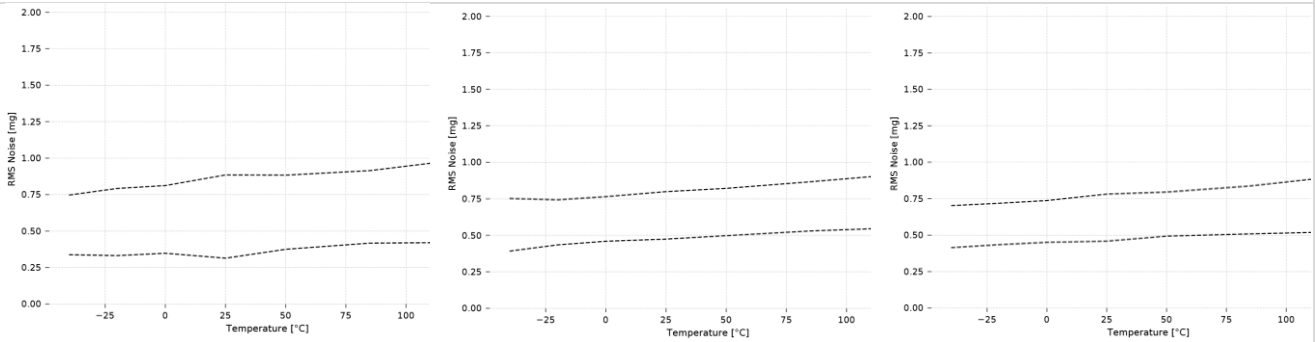
Allan variance 4 σ population limits

3.7 Accelerometer typical performance characteristics

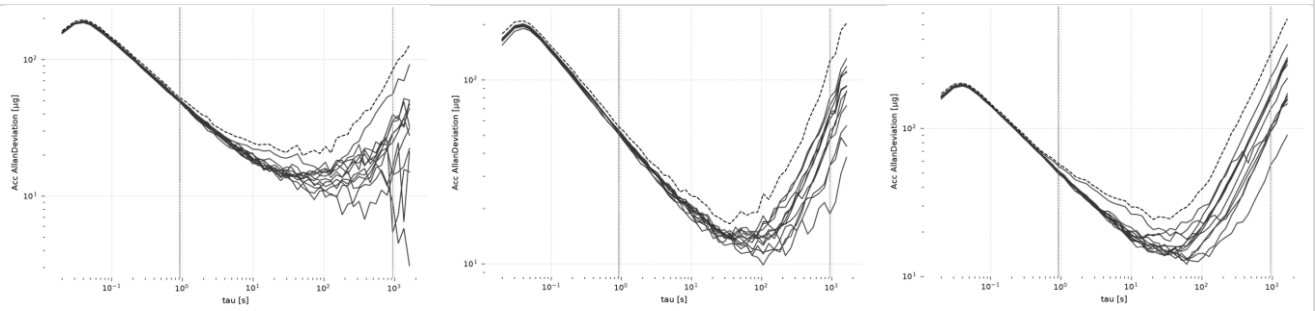
X-Axis Y-Axis Z-Axis



Offset drift over temperature from room temperature (mg) 4 σ population limits



RMS noise 68 Hz LPF (mgRMS) 4 σ population limits



Allan variance 4 σ population limits

3.8 Temperature sensor

Table 8 Temperature sensor performance specification

Parameter	Min	Nom	Max	Unit
Measurement range	-50		135	°C
Temperature signal sensitivity		100		LSB/°C
Total Error	-15		15	°C
Linearity	-1		1	°C

Temperature is converted to °C with following equation:
Temperature [°C] = TEMP / 100, where TEMP is temperature sensor output register content in 2's complement format.

3.9 Gyroscope and accelerometer frequency response and filter characteristics

SCH16T Filter characteristics are presented in table below.

Table 9 SCH16T Filter characteristics

Filter	Title	Type	Order	Min	Nom	Max	Unit
LPF0	Cut-off frequency (-3 dB)	Butterworth	4	63.5	68	72.5	Hz
	Group Delay					10	ms
	Settling time				10	20	ms
LPF1	Cut-off Frequency (-3 dB)	Butterworth	4	28	30	32	Hz
	Group Delay					16	ms
	Settling time				25	40	ms
LPF2	Cut-off Frequency (-3 dB)	Butterworth	3	12.2	13	13.8	Hz
	Group Delay					35	ms
	Settling time				65	200	ms
LPF3	Cut-off Frequency (-3 dB)	Bessel	4	262	280	300	Hz
	Group Delay					1.15	ms
	Settling time					5	ms
LPF4	Cut-off Frequency (-3 dB)	Bessel	3	346	370	394	Hz
	Group Delay					0.78	ms
	Settling time					1.56	ms
LPF5	Cut-off Frequency (-3 dB)	Bessel	3	220	235	250	Hz
	Group Delay					1.24	ms
	Settling time						ms
LPF7	Cut-off Frequency (-3 dB)	None					Hz
	Group Delay						ms
	Settling time					0.78	ms

3.10 Pin description

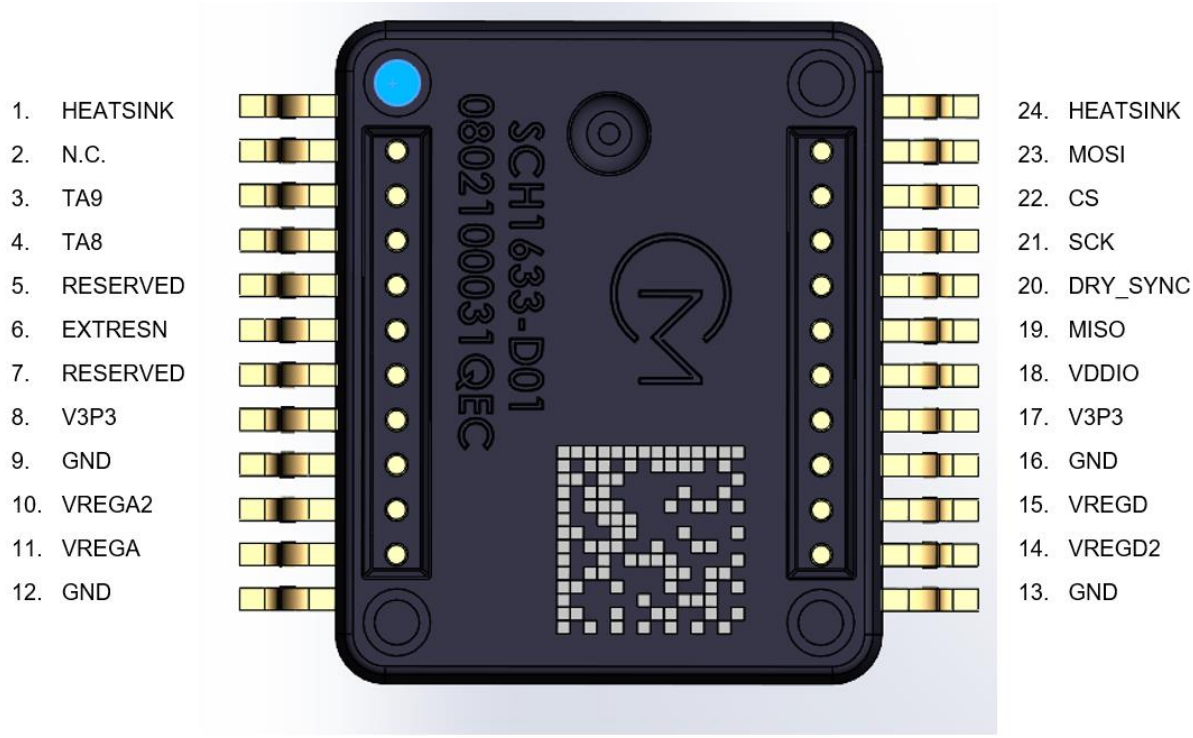


Figure 1 SCH16T pin layout

Table 10 SCH16T Pin description

Pin #	Name	Description	Type	Voltage Level	Default state/structure
1	HEATSINK	Heatsink connection	GND	0 V	
2	Reserved	Leave floating	N/A		
3	TA9	SPI device selection Address 1 (static). Slave addressing in SafeSPI2. Max four slaves can be addresses by TA9:8. TA on the slave is defined by DVIO logic level at pins TA9 and TA8.	DIN	0 V	0/PDR[1)]
4	TA8	SPI device selection Address 0 (static). Slave addressing in SafeSPI2. Max four slaves can be addresses by TA9:8. TA on the slave is defined by DVIO logic level at pins TA9 and TA8.	DIN	0 V	0/PDR[1)]
5	Reserved	Connect to GND	N/A		
6	EXTRESN	External reset input (low active) during normal operation.	DIN/AIN	VDDIO	1/PUR[1)]
7	Reserved	Connect to GND	N/A		

Pin #	Name	Description	Type	Voltage Level	Default state/structure
8	V3P3	External unregulated inputs for the core supply regulators	SUPPLY	3.3 V	
9	GND	Ground	GND	0 V	
10	VREGA2	Regulated core voltage for the analog circuitry. External capacitor connection for positive reference/supply voltage. Connected in PCB.	AIN	2.5 V	
11	VREGA	Regulated core voltage for the analog circuitry. External capacitor connection for positive reference/supply voltage. Connected in PCB.	AOUT	2.5 V	
12	GND	Ground	GND	0 V	
13	GND	Ground	GND	0 V	
14	VREGD2	Regulated core voltage for the digital circuitry. External capacitor connection for positive reference/supply voltage. Connected in PCB.	AIN	1.5 V	
15	VREGD	Regulated core voltage for the digital circuitry. External capacitor connection for positive reference/supply voltage. Connected in PCB.	AOUT	1.5 V	
16	GND	Ground	GND	0 V	
17	V3P3	External unregulated inputs for the core supply regulators	SUPPLY	3.3 V	
18	VDDIO	Digital supply IO	SUPPLY	3.3 V	
19	MISO	Master In Slave Out (SPI)	DOUT	VDDIO	TRI
20	DRY_SYNC	Sync input (active high) DRY (Data Ready) outputs an interrupt signal for external MCU when the internal output registers (gyroscope + accelerometer) have been updated.	DIN/DOUT	VDDIO	0/PDR
21	SCK	Serial clock (SPI)	DIN	VDDIO	0/PDR
22	CS	Chip select (SPI)	DIN	VDDIO	1/PUR
23	MOSI	Master Out Slave In (SPI)	DIN	VDDIO	0/PDR
24	HEATSINK	Heatsink connection	GND	0 V	

1) Strong PD/PU resistance during device reset state, otherwise weak PD/PU.

3.11 Digital I/O specification

Table 11 SPI DC characteristics describes DC characteristics of the SCH16T sensor SPI I/O pins. Current flowing into the circuit has a positive value.

Table 11 SPI DC characteristics

Title	Symbol	Min	Max	Unit
SPI Voltage Level	VIO	1.7	3.6	V
Input High Voltage	VIH	0.7*VIO	VIO	V
Input Low Voltage	VIL	0	0.3*VIO	V
Input Voltage Hysteresis	VHYST	0.1*VIO		V
Input/Output Capacitance	CIO		10	pF
Total MISO load capacitance, <Wide> range	CLWIDE	10	100	pF
Input pull-down resistance, strong (default)	RPD	60	140	kOhm
Input pull-up resistance, strong (default)	RPU	60	140	kOhm
Input pull-down/pull-up resistance, weak (option)	RPD/RPU	200	400	kOhm
Output leakage current in case MISO is in high impedance (tri-state) condition	ILEAK	-10	10	µA

3.12 SPI AC characteristics

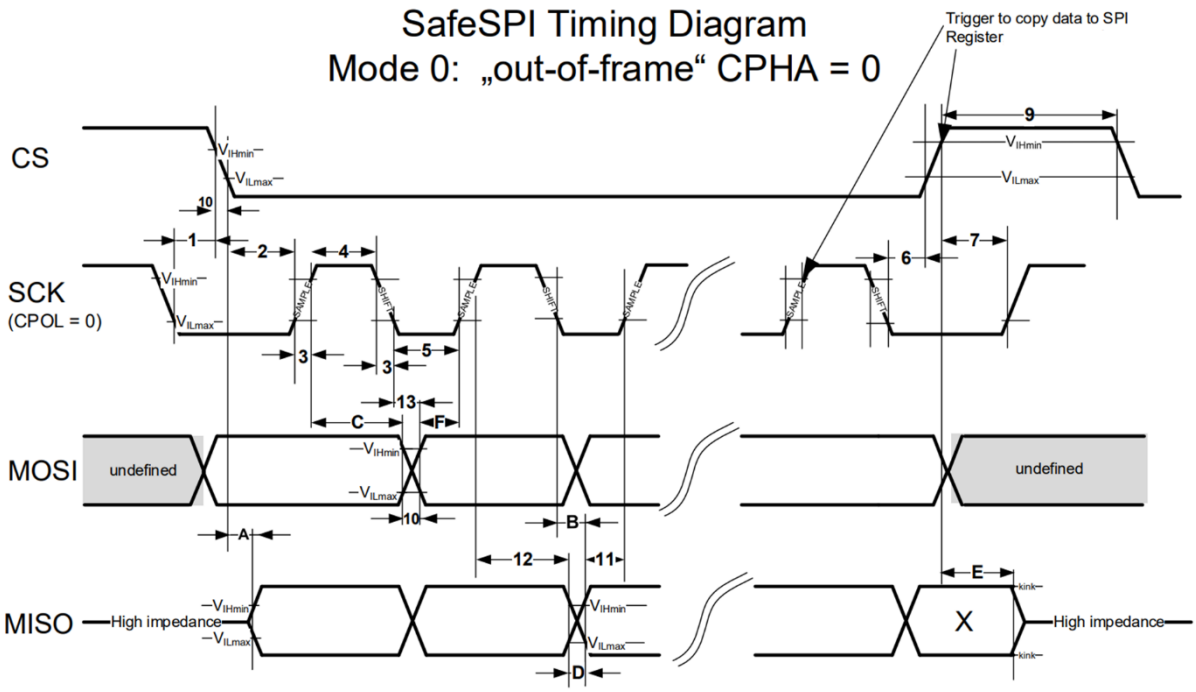


Figure 2 Timing diagram of SPI communication (SPI mode 0), CPOL = 0, CPHA = 0

Table 12 SPI AC electrical characteristics

Title	Remark	Symbol	Min	Max	Unit
SCK Operating Frequency			0.095	10.5	MHz
MISO data valid time (CS)		A		40	ns
MISO data valid time (SCK)		B		32	ns
MOSI data hold time		C	20		ns
MISO rise/fall time	MISO rise/fall time is not defined during transition between high impedance and active mode	D	2	9	ns
MISO data disable lag time		E		50	ns
MOSI data setup time		F	10		ns
SCK disable lead time		1	10		ns
SCK enable lead time		2	40		ns
SCK rise and fall time		3	2	9	
SCK high time		4	37		ns
SCK low time		5	37		ns
SCK enable lag time		6	20		ns
SCK disable lag time		7	10		ns
Sequential transfer delay	In case of MOSI Write commands (RW=1)	9	750		ns
Sequential transfer delay	In case of MOSI Read commands (RW=0)	9	450		ns
MOSI rise and fall time		10	2	9	ns
MOSI data setup time	Setup time of MOSI before the rising edge of SCK	11	5		ns
MISO data hold time		12	X		ns
MOSI valid time		13		10	ns
CS rise and fall time		10	2	9	ns

3.13 Measurement axis and directions

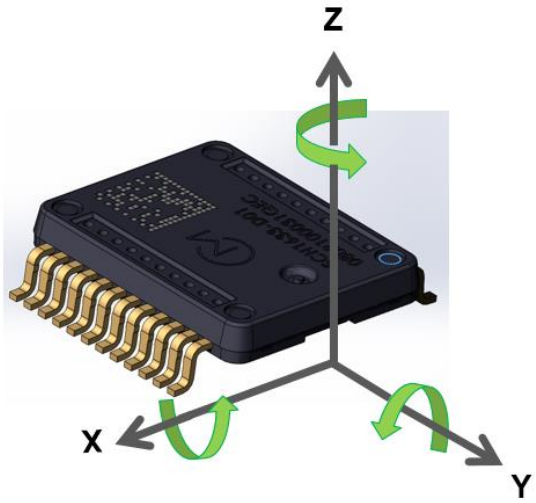


Figure 3 SCH16T measurement directions for gyroscope and accelerometer

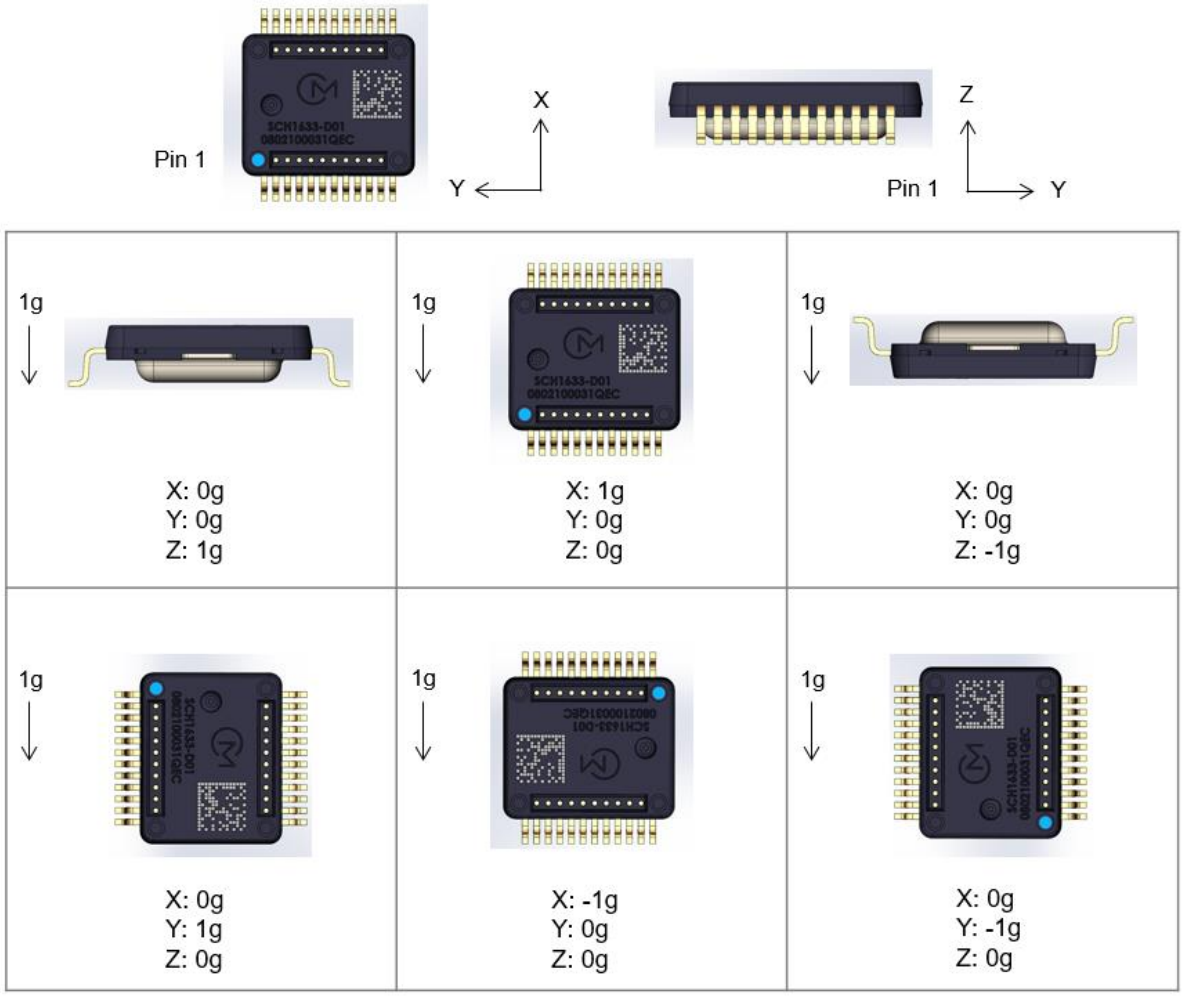


Figure 4 SCH16T accelerometer measurement directions and outputs. 1g indicates direction of gravity. Note: Pin 1 is marked in blue only in this data sheet to emphasize location.

3.14 Package outline drawing

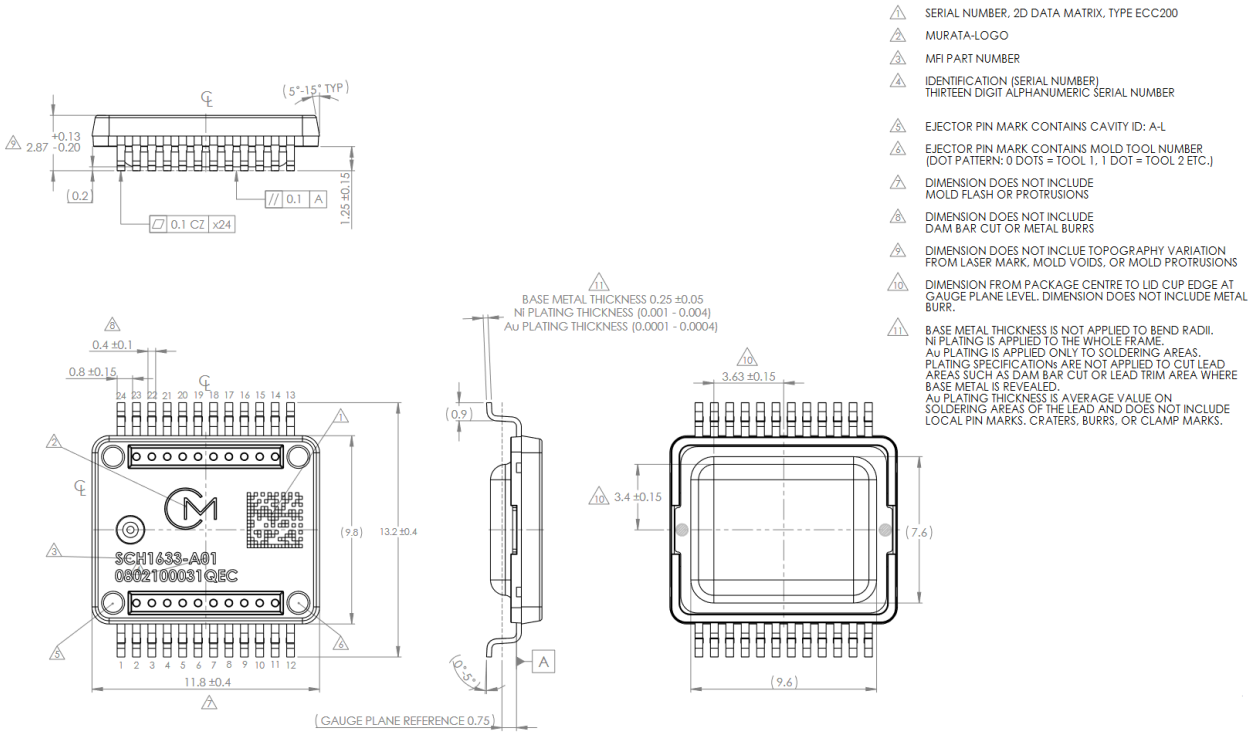


Figure 5 The outline of SCH16T package. All dimensions are in millimeters. All angles are in degrees. Tolerances unless otherwise specified according to ISO2768-f. This figure is preliminary and will be updated later.

3.15 PCB footprint

SCH16T PCB footprint dimensions are presented in the table below.

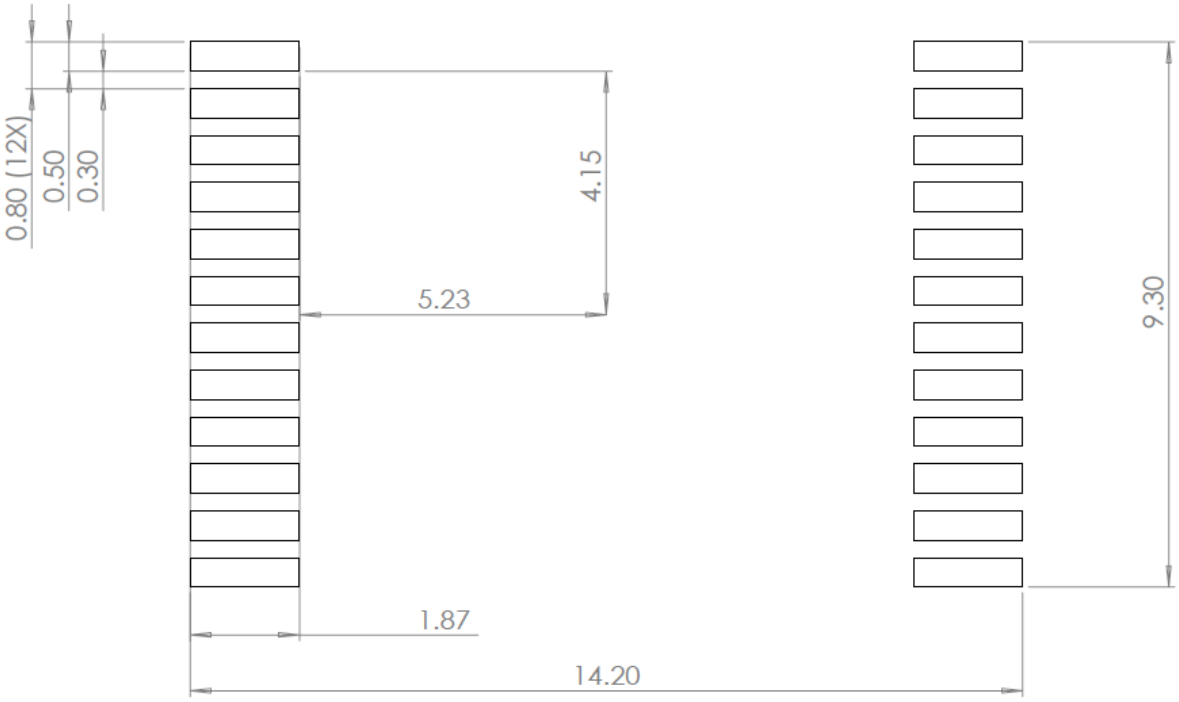


Figure 6 Recommended PCB pad layout for SCH16T. All dimensions are in millimeters.

This is the end of publicly available document. For full version of this of this data sheet and assembly instructions, please contact Murata.

4 General product description

4.1 Component block diagram

The SCH16T sensor consists of independent acceleration and angular rate sensing elements, and an Application-Specific Integrated Circuit (ASIC) used to sense and control those elements. The angular rate and acceleration sensing elements are manufactured using Murata's proprietary High Aspect Ratio (HAR) 3D-MEMS process, which enables making robust, extremely stable, and low noise capacitive sensors.

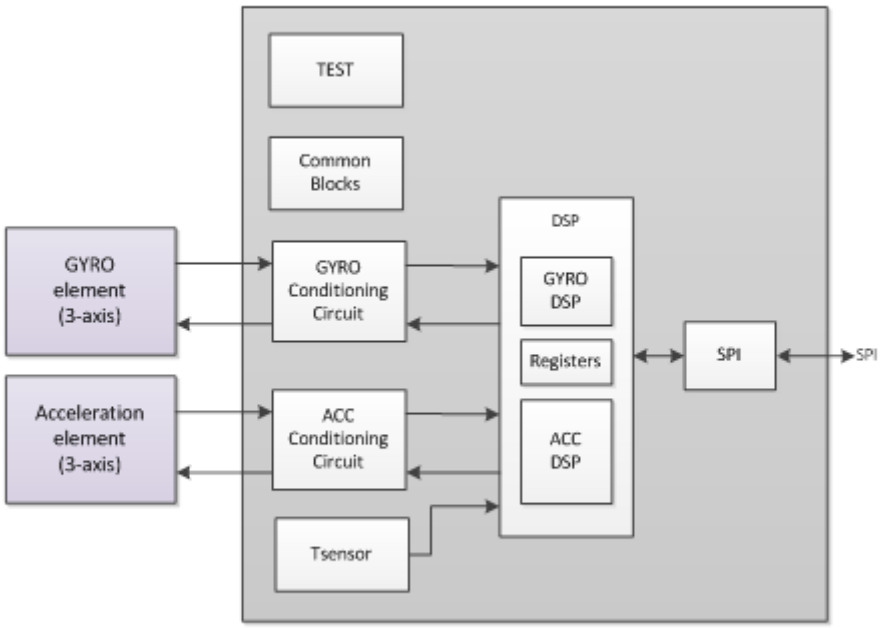


Figure 7 SCH16T Component block diagram

4.2 Accelerometer

The acceleration sensing element consists of three acceleration-sensitive masses. Acceleration causes a capacitance change that is converted into a voltage change in the signal conditioning ASIC.

4.3 Gyroscope

The angular rate sensing element consists of moving masses that are intentionally exited to in-plane drive motion. Rotation in a sensitive direction causes in-plane (Z) or out-of-plane (XY) movement that can be measured as capacitance change with the signal conditioning ASIC.

4.4 Factory calibration

Sensors are factory calibrated and there is no need for separate calibration in most applications. Factory calibrated parameters include offset, sensitivity, internal fault monitoring signals and cross-axis sensitivity for gyroscope and accelerometer.

Sensors are calibrated over temperature in three measurement points at -40 °C, +25 °C, and +110 °C. Offset and sensitivity are calibrated with 2nd order polynomial and cross-axis with linear function. Calibration variables are stored in non-volatile memory during manufacturing and are read automatically during the start-up.

It should be noted that PCB assembly can cause offset errors to the sensor output. If possible, system-level offset calibration (zeroing) after assembly is recommended.

5 Component operation, reset and power-up

5.1 Component operation

The SCH16T component has an internal power-on reset circuit. After release of EXTRESN and once the power supplies are within the specified range, the component reads configuration and calibration data from the non-volatile memory to volatile registers. After the memory is read, the sensor goes to low power mode and an external SPI command, EN_SENSOR, is needed to continue to the initialization phase and to start the measurement.

Start-up time is dependent on the low pass filter setting. After power-on or reset (release of EXTRESN or EN_SENSOR command) the sensor shall be able to provide valid acceleration and angular rate data after the specified power-on start-up time.

SCH16T uses LPF0 (68 Hz) low pass filter setting by default and the filter can be changed by SPI command. SCH16T has extensive internal fault diagnostics to detect possible over range and internal failures. Diagnostic status can be monitored via status bits included in SPI frame and status registers.

5.2 Internal fault diagnostics

During the startup sequence, the sensor performs a series of internal tests that will set various error flags in the sensor status registers. To clear them it is necessary to read the status registers after the start-up sequence is complete. When reading the status registers, the user must consider that the state of status flags is not defined during LPM (Low Power Mode) and the 250 ms wait state after EN_SENSOR.

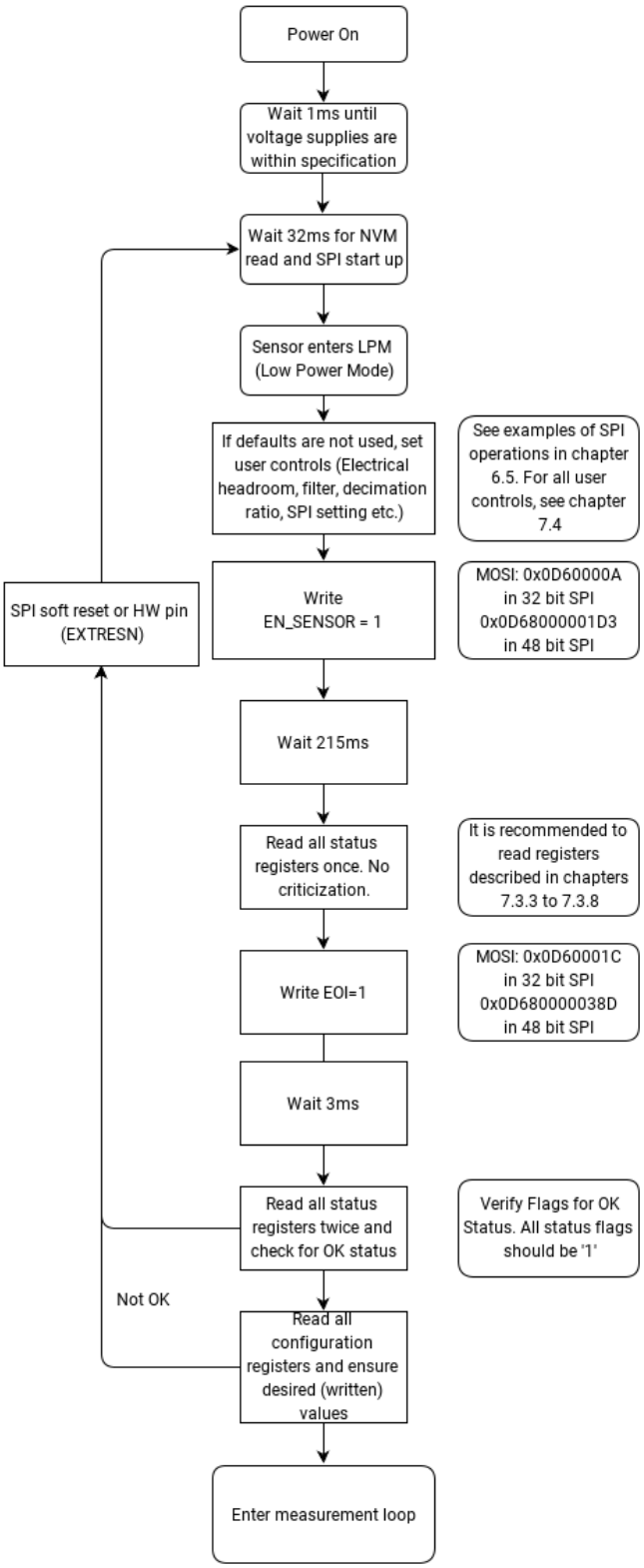


Figure 8 Example of SCH16T start-up sequence

5.3 Component output channels

The SCH16T series component has several output channels for the user to choose from. The component has two channels for reading gyroscope data and a total of 3 channels for reading acceleration data. Each channel consists of separate X, Y and Z output data registers and each channel and axis has separate status flags. The first gyroscope data channel RATE_XYZ1 has interpolated output and the second channel RATE_XYZ2 is for decimated output. The first acceleration channel ACC_XYZ1 has interpolated output, second channel ACC_XYZ2 is for decimated output and the third channel is an auxiliary interpolated channel, ACC_XYZ3. Interpolation and decimation are explained in more detail in 5.4.
The user may choose to utilize multiple channels simultaneously and adjust channel settings separately according to the users' needs. Dynamic range can be individually set for each channel, but filter settings are shared between interpolated and decimated outputs. Different filters within one channel can be applied between X-, Y- and Z-axis, if desired. For example, the user can read ACC_XYZ1 with nominal ±163.4 m/s^2 dynamic range and 68 Hz filter, and ACC_XYZ3 with nominal ±20.48 m/s^2 dynamic range and 13 Hz filter. The output options are presented in the table below.

Table 13 SCH16T output channel options

Channel	Description	Filter setting	Dynamic range setting
RATE_XYZ1	Interpolated gyroscope output	Common for both gyro channels, selectable separately for each axis	RATE_XYZ1 specific
RATE_XYZ2	Decimated gyroscope output		RATE_XYZ2 specific
ACC_XYZ1	Interpolated accelerometer output	Common for ACC_XYZ1 and ACC_XYZ2 channels, selectable separately for each axis	ACC_XYZ1 specific
ACC_XYZ2	Decimated accelerometer output		ACC_XYZ2 specific
ACC_XYZ3	Auxiliary interpolated accelerometer output	ACC_XYZ3 specific, selectable separately for each axis	ACC_XYZ3 specific

5.4 Solutions for asynchronous clock domains

Multiple features are implemented to improve synchronization between the product's internal clock and application system clock. While most systems can most likely cope with conventional continuous polling of SPI peripheral, accurate time-domain synchronization can be essential in certain high-performance applications. The table below summarizes the synchronization features.

Table 14 Solutions for asynchronous clock domains

Feature	Use case	Value
Interpolation	This should be used by default. Interpolation is applied in outputs RATE_XYZ1, ACC_XYZ1, and ACC_XYZ3.	- Minimized sampling jitter - Minimized timing difference between channels - No missing samples
SYNC Input	Special case. Recommended if there is a need to sync between multiple SCH16T family sensors or if sample time consistency is valued over jitter	- Synchronization between multiple sensors. - Data can be received with consistent rate even if host system sampling is affected by changing load
DRY Output (Data Ready Interrupt)	Special case. Recommended only if decimated, low update rate outputs RATE_XYZ2 and ACC_XYZ2 are used. Decimated outputs are typically used if MCU bandwidth is limited.	- Minimized sampling jitter. With decimated outputs, the maximum data jitter depends on the decimation ratio and interrupt use removes this jitter totally. - No missing samples.
Data counter	Special case. Recommended only if Data Ready is not preferred in application.	- Data counter is index for the component data output values. The application can monitor that:

Feature	Use case	Value
		- Data is updating - Every wanted sample has been acquired - The same sample has not been read twice
Data counter with frequency counter	Special case. Recommended if integration operation is performed to sensor data and timing uncertainty or data jitter of the interpolated data do not fulfill the system accuracy requirements.	- Data counter together with frequency counter can be used for more accurate integration.

SYNC and DRY (Data Ready) are implemented on a single hardware pin. Therefore, simultaneous use of these functions is not possible. Controlling the behavior of SYNC and DRY is explained in chapter *7.4*.

5.4.1 Interpolation

The purpose of interpolation is to minimize time uncertainty (sampling jitter) by increasing artificially the internal sample rate. The natural output data rate of all data outputs is F_PRIM/2, which is 11.8 kHz with nominal primary frequency. This means that a time-uncertainty between sensor register update and system sampling time could be theoretically anything between 0...85 µs.
To minimize this jitter, a fixed interpolation factor of 32 is applied to outputs RATE_XYZ1, ACC_XYZ1, and ACC_XYZ3. With nominal primary frequency it corresponds to a 377.6 kHz refresh rate of register content.
The sample rate is increased by adding a one(1) cycle latency delay to the initial sample. The delay corresponds to the maximum time uncertainty which with nominal primary frequency is 85 µs. A linear interpolation is then applied between the initial sample and the new sample, and this interpolation is divided into time segments by the artificially increased update rate 32 x F_PRIM/2. Time uncertainty is now reduced to the length of this segment, which is max (85 µs)/32 = 2.6 µs (with nominal primary frequency).

Please refer to illustration below.

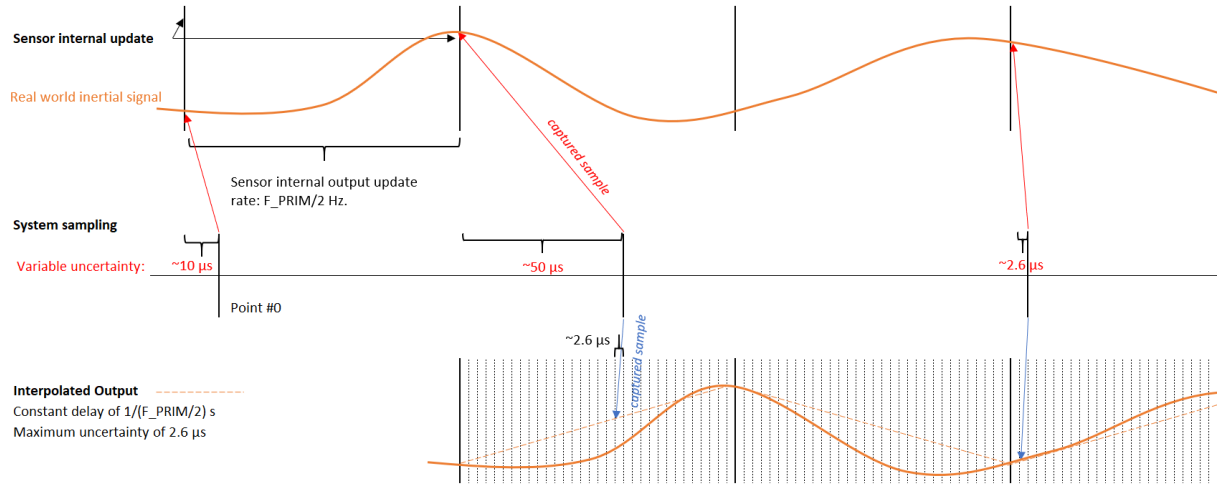


Figure 9 Interpolation (8kHz system sampling rate is used in this illustration)

5.4.2 Decimation

Certain systems need to utilize every available sample and for example acquire samples from all axis at the same time instant. As the natural output data rate with nominal primary frequency is 11.8 kHz, this can create excessive load for the MCU. The purpose of decimation is to decrease the internal update rate to give the host system enough time to read every sample.
During start-up, the user can select a suitable decimation from the options presented in Table 15 Selectable decimation ratios and corresponding ODR. The selected decimation ratio is applied to outputs RATE_XYZ2 and ACC_XYZ2.

Table 15 Selectable decimation ratios and corresponding ODR

Decimation factor	Output data rate	Output data rate with nominal F_PRIM (kHz)
1	F_PRIM/2	11.8
2	F_PRIM/4	5.9
4	F_PRIM/8	2.95
8	F_PRIM/16	1.475
16	F_PRIM/32	0.7375

Drawback of decimation is that sampling jitter is increased with the same ratio as the decimation factor. With nominal primary frequency and decimation ratio of 16, the sampling jitter will be up to 85 µs x 16 = 1.36 ms. This means that sample age can be anything between 0 and 1.36 ms. To address this issue, the user can combine decimation with the data ready function. Data ready is explained in chapter 5.4.4.

5.4.3 SYNC input pin

Certain systems with high-performance requirements may benefit from use of multiple SCH16T components. Depending on application SPI master clock conditions, the read operation of multiple parallel sensors can take longer than sensor internal register update period if individual MISO line is not used for each component. As a result of this, samples are being acquired from different time instants for each parallel sensor. In certain real-world inputs, this can lead to a significant apparent disagreement of sensors, as different time-instants are being sampled.
To mitigate this issue, SYNC input pin has been implemented. When the master issues SYNC signal to all sensors in the system, the sensors' internal updates for RATE_XYZ1/2 and ACC_XYZ1/2/3 are frozen until SYNC pin is set LOW, or after time out period set by CTRL_SYNC_TOC_TH time-out counter. This allows enough time for the master to read all sensor data from a single time instant. CTRL_SYNC_TOC_TH is user-selectable with typical values ranging from 1.2 ms to 11.6 ms. Please refer to chapter 0 for user controls.

SYNC is only feasible on interpolated outputs RATE_XYZ1 and ACC_XYZ1/3. With decimated outputs and a decimation factor of 2 or above, most masters should have enough time to read the output registers before they are updated again.

SYNC can be beneficial also to ensure that all 6-axis data is captured at the same time instant. With very low SPI master clocks, it can occur that even a single sensor will update its internal registers during the slow read operation. In this case, different axis data could represent different time instant. SYNC can also help in situations where system load is high, and sampling can not be performed with a consistent frequency.

Please refer to illustration below.

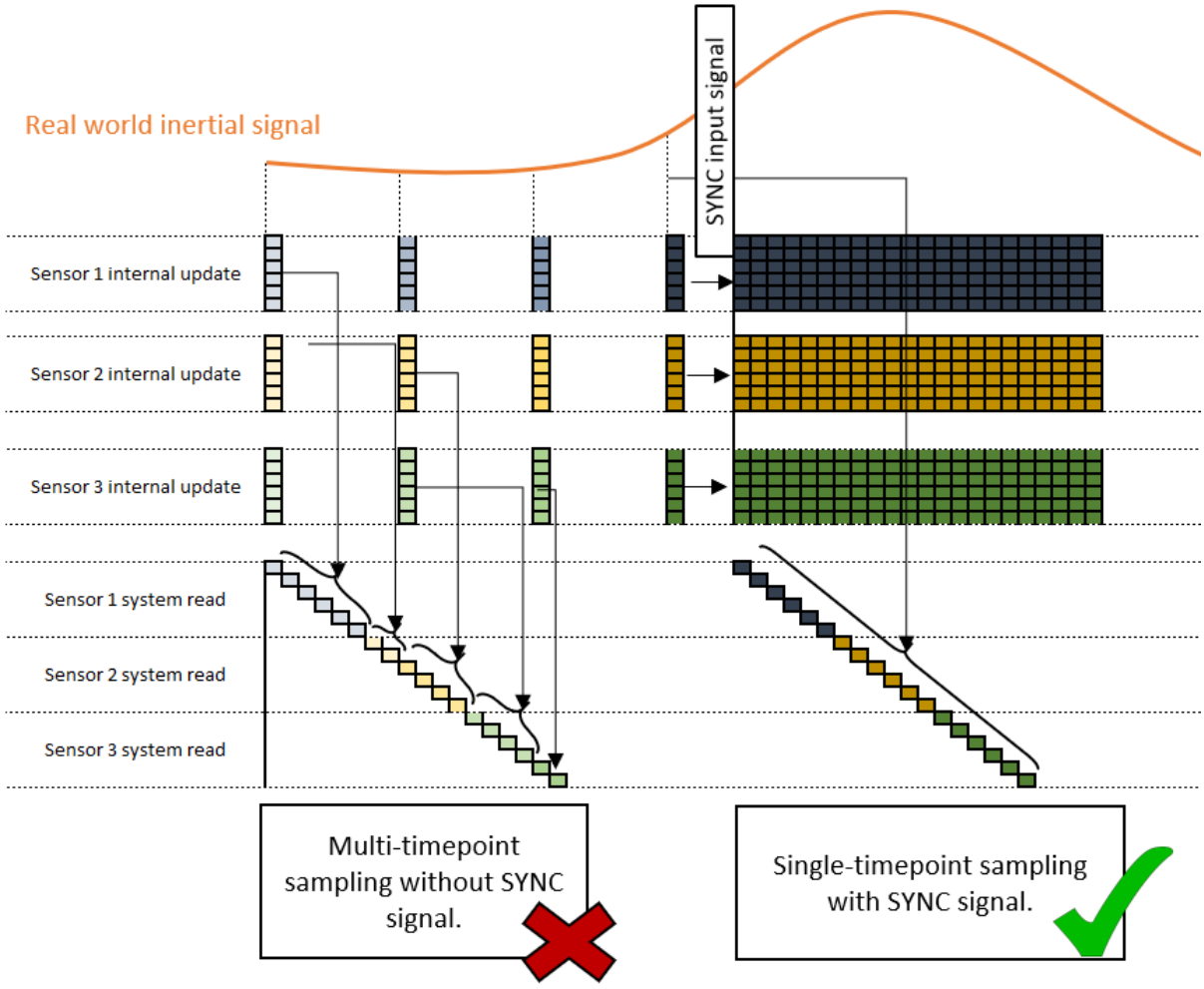


Figure 10 Illustration of SYNC usage when 3 slave sensors are read by single a master

5.4.4 Data ready, DRY

In some system implementations, it may be that the rate at which the host processor can read the peripherals is limited. In these cases, to ensure that the host has enough time to read without signal aliasing it is beneficial to use decimated outputs with suitable decimation factor. When the sensor update rate is lowered by decimation, sampling jitter becomes more of an issue. As explained in chapter 5.4.1, worst case sampling jitter can be up to 85 µs with decimation factor of 1. When decimation factor is increased, the worst-case sampling jitter is increased accordingly.

In case jitter minimization is critical in application, user should use the data ready output pin (DRY_SYNC). When all sensor output channels have been updated, the data ready triggers a rising edge to indicate that the samples were generated. This rising edge can be used as a direct interrupt to start sensor read operation, or the host can take note of the data ready signal and ensure that the data is read in a burst before the next expected sensor internal update. This way the system can ensure that no samples are missed, and no samples are being read twice.

Please refer to illustration below.

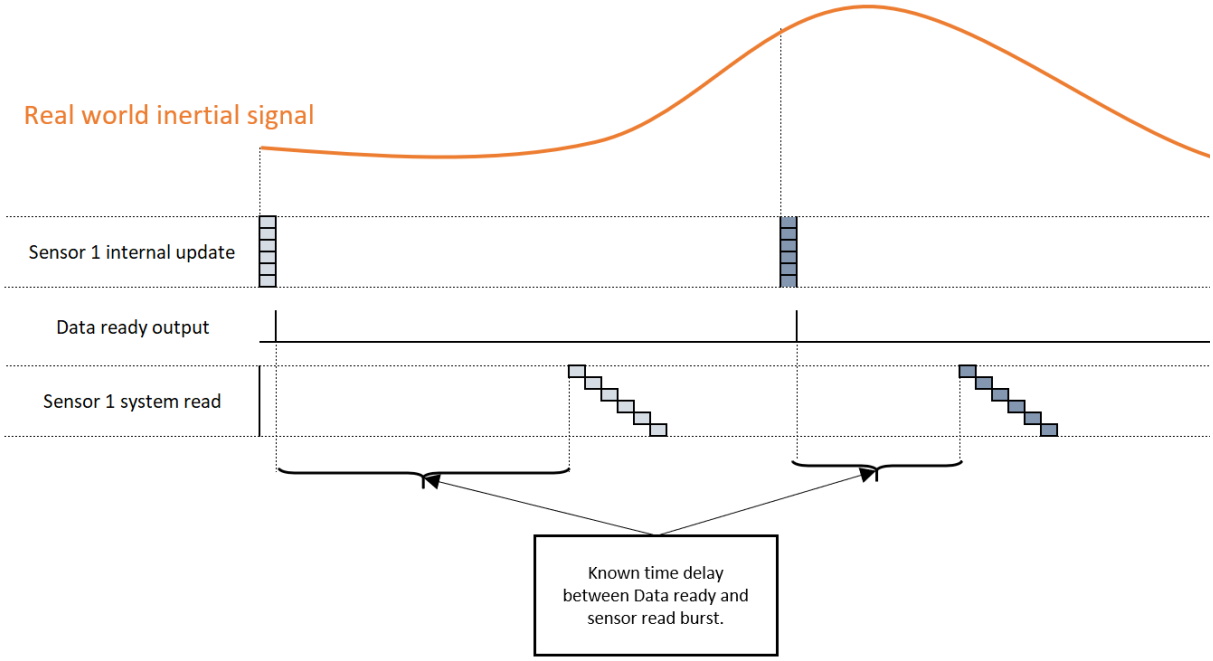


Figure 11 Illustration of data ready output signal. In this example, data is read in a burst between sensor internal updates.

5.4.5 Data counter

Data counter is supported for decimated outputs RATE_XYZ2 and ACC_XYZ2. Value of data counter is increased by one when a new sample is available from corresponding RATE/ACC channel. It can be understood as an index for the data output values. Using the data counter, the user can monitor that every wanted sample has been acquired and that the same sample has not been read twice.
When using 48-bit SPI protocol, 4-bit data counter value is included in MISO response frame. Data counter can be also used in 32-bit mode by reading DCNT_RATE and DCNT_ACC register values via SPI command. Register locations are described in chapter *7.3*.

5.4.6 Frequency counter

Using frequency counter, user can acquire accurate clock information from component internal MCLK via SPI. The value of frequency counter register is increased by one with every 16th rising edge of master clock.

5.4.7 Calculating exact time stamp

The data counter value can be combined with the frequency counter value to calculate the exact time stamp of a sample when the MCU clock of the host system is used as reference. This combination is recommended if integration operations are performed to sensor data and timing uncertainty or data jitter of the interpolated data do not fulfill system accuracy requirements.

6 Component interfacing

6.1 Safe SPI

Product supports Safe SPI v2.0 protocol to transfer data between SPI master and registers of SCH16T ASIC. The product always operates as a slave device in master-slave operation mode. 3-wire SPI connection cannot be used. Communication between master and slave is done with pins described below in Table 16 SPI interface pins.

Table 16 SPI interface pins

SPI interface pin	Description	Communication direction
CS	Chip Select (active low)	MCU to ASIC
SCK	Serial Clock	MCU to ASIC
MOSI	Master Out Slave In	MCU to ASIC
MISO	Master In Slave Out	ASIC to MCU

SPI communication uses out-of-frame protocol, so each transfer has two phases. The first phase contains the SPI command (request) and the data (response) of the previous command. The second phase contains the next request and the response to the request of the first phase, see Figure 12. The first response after reset is undefined and shall be discarded.

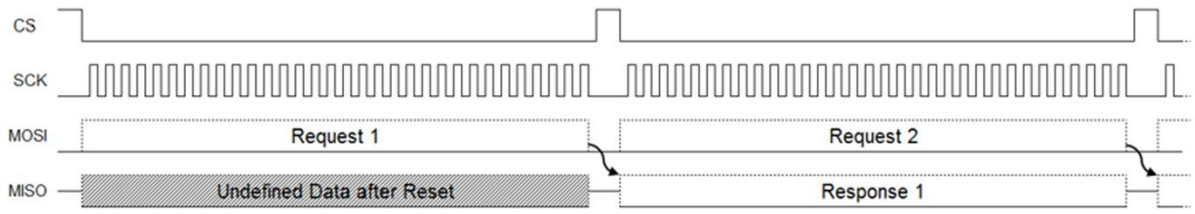


Figure 12 SPI protocol example

Product SPI block implements two different SPI protocol types. Both protocol types can be used during operation by defining the SPI frame bit length.

- SafeSPI2 32-bit frame, SPI32BF.
- SafeSPI2 48-bit frame, SPI48BF.

SPI block does not implement the complete SafeSPI v2.0 specification. Summary of supported features can be seen in table below. For Safe SPI standard, please refer to www.SafeSPI.org

Table 17 SCH16T supported features of SafeSPI v2.0

Supported feature	Description
<48/32oof>	Block receives and transmits 32-bit and 48-bit Out-of-frame SPI frames. In-frame protocols are not supported.
<FrTyp>	MOSI frame width is defined by received frame length. Frame is effective only if width is 32-bits or 48-bits and the CRC is valid.
<SelBitWidthByAdr >	Next MISO frame width is decided by <FrTyp>
<Sel4SlaveByAdrPin>	Two MSB address bits can be used to select one of four slaves when one CS signal pin is in use. Slave compares the two MSBs to a reference value defined by two input pins.
<Sel4SlaveByAdrNVM>	Two MSB address bits can be used to select one of four slaves when one CS signal pin is in use. Slave compares the two MSBs to a reference value defined by a NVM programmed value. Factory use only.
<FixedSensorFrame>	Frame content is well defined and fixed.
<CLWide>	Wide range for “total signal load capacitance”
<DCnt>	Block updates a wrapping 4-bit sample counter each time new sensor data is generated.
<IDS>	Internal Data Status field includes additional status information for sensor data.
<CAP>	Not implemented and replaced with fixed value.

The SPI transmission is always started with the CS falling edge and terminated with the CS rising edge. The data is captured on the SCK's rising edge (MOSI line) and it is propagated on the SCK's falling edge (MISO line). This equals to SPI Mode 0 (CPOL = 0 and CPHA = 0), an example with 32-bit frame can be seen in Figure 13 SPI frame format example (32-bit).

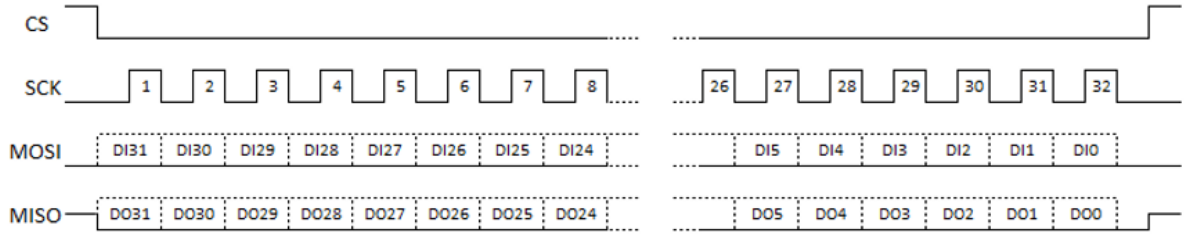


Figure 13 SPI frame format example (32-bit)

6.2 SPI frame structure

SPI Frame format is explained in figure below and *Table 18 SPI bit definitions*

SPI48BF

Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	TA 9:0										RW	0	FT	AE							DATAI 19:0																				CRC8							
MISO (sensor data)	D	SA 9:0										IDS	CE	S1:0			DCNT			*	SENSOR 19:0																				CRC8							
MISO (other data)	D	SA 9:0										IDS	CE	S1:0			*				INFO 19:0																				CRC8							

SPI32BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	TA 9:0										RW	0	FT	DATAI 15:0																CRC3		
MISO (sensor data)	D	SA 9:0										S1	SENSOR 15:0																S0	CRC3		
MISO (other data)	D	SA 9:0										S1	INFO 15:0																S0	CRC3		

Figure 14 SPI frame format for 48-bit and 32-bit frames

Table 18 SPI bit definitions

SYMBOL	DESCRIPTION
D	D=1 condition: Gyro data register read ACC data register read Temperature data register read D=0 condition: Any other register than listed above is read
TA	Defines the Target Address in SCH16T. TA[9:8] bits are used as Chip Select information, and thus they are not part of the effective address. TA[7:0] are used as effective address within the chip.
SA	Contains the Source Address. It has the same content as TA.
RW	Read/write access selector. Read is selected with 0 and write with 1.
FT (FrTyp)	Frame Type for next MISO frame: 0 for SPI32BF, 1 for SPI48BF. MOSI frame width is defined by the MOSI frame itself, hence this field should match the next incoming MOSI frame since out-of-frame responses are in use.
AE	Reserved. Bits shall be ignored.
DATAI	MOSI line input data from SPI host. This field is 20-bits wide for SPI48BF and 16-bits for SPI32BF.
SENSOR	MISO line sensor type output data towards SPI host.
INFO	MISO line non-sensor type output data towards SPI host. This field is 20-bits wide for SPI48BF and 16-bits for SPI32BF. 20-bit data is clipped from LSB end to 16-bit with SPI32BF, i.e. data is MSB aligned.
*	Unused field that is ignored for receive and set to all-zeros for transmit.
S1:0, S1, S0	Sensor status indication.
CE	Command Error indication. SCH16T reports only semantically invalid frame content using this field. SPI protocol level errors are indicated with High-Z on MISO pin.
IDS	Internal Data Status indication. SCH16T uses this field to indicate common cause error. This is redundant, more

SYMBOL	DESCRIPTION
	accurate info is seen from sensor status (S1:S0).
DCNT	A wrapping 4-bit sensor data counter.
CRC8 (C7:0)	8-bit CRC reference for SPI48BF. Calculated over bits 47 to 8.
CRC3 (C2:0)	3-bit CRC reference for SPI32BF. Calculated over bits 31 to 3.

6.3 Multi-slave operation

SCH16T SPI supports several slave devices on single bus by using either multiple chip select lines, one for each slave, or with one common chip select (CS) and using TA9 and TA8 pins to enable logical addressing.

Pin 3 (TA9) and pin 4 (TA8) correspond to the bits TA9:9 and TA8:8 included in the SPI MOSI frame. Issuing a pull-up signal to either pin means that the components TA bit has been flipped as ‘1’ in component logic level. All options for addressing four slaves are shown in figure below.

Example: Compose MOSI frame targeted to component #3
1. Set pin 3 (TA9) low and pin 4 (TA8) high
2. Send MOSI frame in which TA9:8 is written as ‘01’

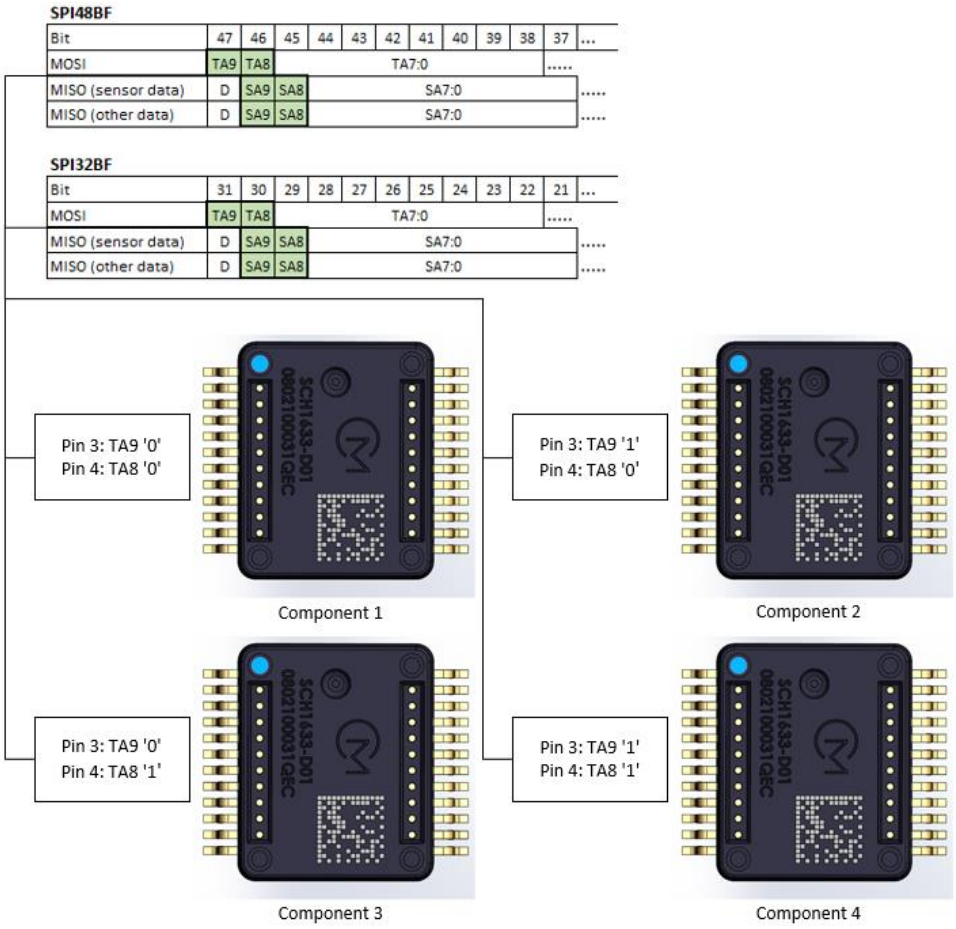


Figure 15 Multi-slave operation

6.4 SPI frame status bits

Status bits indicate functional status of the sensor. See table below for definitions of bits S[1:0]

Table 19 Status bit description

Status bits S[1:0]	Description
00	Normal operation
01	Error status
10	Saturation error
11	Initialization running

S[1:0] priority order is 11 (Initialization) --> 01 (Error) -->10 (Saturation) --> 00 (Normal operation)

Note that the Status bits S[1:0] are always '00' on the response frame for register write commands.

IDS, or Internal Data Status bit is redundant error status bit for S[1:0] in case of common status error.
0 - Normal Operation
1 - Common Error

CE status bit reports Command Errors.
0 - Normal Operation
1 - Command Error

The following access errors are detected and reported:

- Write request when EOI is active, excluding write to reset activation register.
- Read or write to SPI_TMODE addresses when SPI_TMODE is inactive. (Factory only)
- Read or write request to unused/undefined address.
- Write request to read-only register.

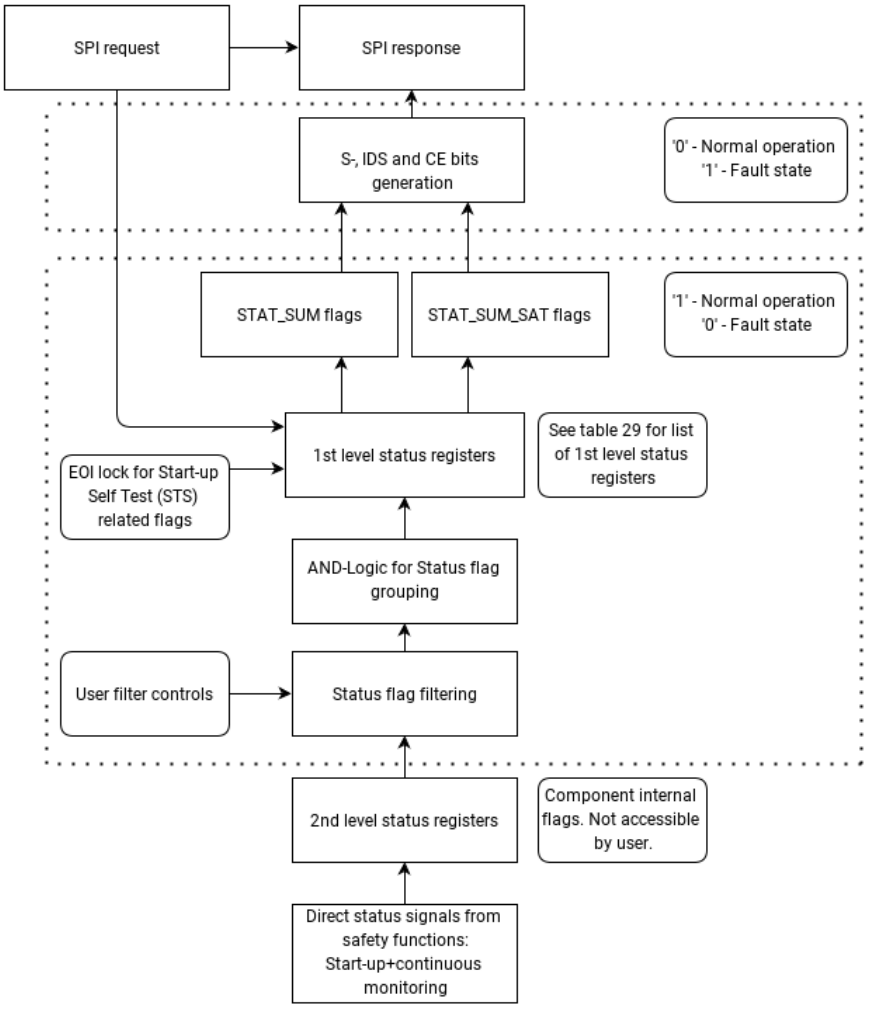


Figure 16 Status flag flow chart

6.5 Cyclic redundancy check (CRC)

6.5.1 SPI48BF CRC

SPI48BF uses 8-bit CRC (CRC8). CRC is calculated from MSB towards LSB for 40 MSB bits of the frame, i.e., from bit 47 to 8. Generator polynomial is b100101111 (POLY:9) and calculation is initialized to b11111111. Final CRC is the direct value of the calculation.

Table 20 CRC definition for 48-bit frames

Parameter	Value
Name	CRC-8
Width	8-bit
Poly	12F'h (generator polynom: $X^8+X^5+X^3+X^2+X+1$) 97'h (Koopman)
Initial	FF'h

6.5.2 SPI32BF CRC

SPI32BF uses 3-bit CRC (CRC3). CRC is calculated from MSB towards LSB for 29 MSB bits of the frame, i.e., from bit 31 to 3. Generator polynomial is b1011 (POLY:4) and calculation is initialized to b101. Final CRC is the direct value of the calculation.

Table 21 CRC definition for 32-bit frames

Parameter	Value
Name	CRC-3
Width	3-bit
Poly	B'h (Generator polynom: X^3+X+1) 5'h (Koopman)
Initial	5'h

6.6 Operations

This chapter describes some common SPI operations.

6.6.1 32-bit mode operations

The SPI binary frame is constructed as follows:
(TA9 TA8 TA[7:0] RW 0 FrTyp DATA[15:0] CRC3)

Table 22 32-bit mode operations and their equivalent SPI frames

Command	Register	SPI Binary Frame	SPI Hex frame
EN_SENSOR	CTRL_MODE	0 0 00110101 1 0 0 0000000000000001 010	0x0D60000A
EOI	CTRL_MODE	0 0 00110101 1 0 0 0000000000000011 100	0x0D60001C
Set LPF0 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 0 0000000000000000 110	0x09600006
Set LPF0 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 0 0000000000000000 000	0x09A00000
Set LPF1 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 0 0000000001001001 100	0x0960024C
Set LPF1 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 0 0000000001001001 010	0x09A0024A
Set LPF2 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 0 0000000010010010 010	0x09600492
Set LPF2 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 0 0000000010010010 100	0x09A00494
Set LPF3 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 0 0000000011011011 000	0x096006D8
Set LPF3 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 0 0000000011011011 110	0x09A006DE
Set RATE Dynamic Range to ±315°/s	CTRL_RATE	0 0 00101000 1 0 0 0010010000000000 000	0x0A212000
Set ACC Dynamic Range to ±80m/s^2	CTRL_ACC12	0 0 00101001 1 0 0 0010010000000000 010	0x0A612002
Read RATE LPF setting	CTRL_FILT_RATE	0 0 00100101 0 0 0 0000000000000000 111	0x09400007
Read ACC LPF setting	CTRL_FILT_ACC12	0 0 00100110 0 0 0 0000000000000000 001	0x09800001
Read RATE_X1	RATE_X1	0 0 00000001 0 0 0 0000000000000000 001	0x00400001
Read RATE_Y1	RATE_Y1	0 0 00000010 0 0 0 0000000000000000 111	0x00800007
Read RATE_Z1	RATE_Z1	0 0 00000011 0 0 0 0000000000000000 101	0x00C00005
Read ACC_X1	ACC_X1	0 0 00000100 0 0 0 0000000000000000 000	0x01000000
Read ACC_Y1	ACC_Y1	0 0 00000101 0 0 0 0000000000000000 010	0x01400002
Read ACC_Z1	ACC_Z1	0 0 00000110 0 0 0 0000000000000000 100	0x01800004
Read ACC_X3	ACC_X3	0 0 00000111 0 0 0 0000000000000000 110	0x01C00006
Read ACC_Y3	ACC_Y3	0 0 00001000 0 0 0 0000000000000000 101	0x02000005
Read ACC_Z3	ACC_Z3	0 0 00001001 0 0 0 0000000000000000 111	0x02400007
Read RATE_X2	RATE_X2	0 0 00001010 0 0 0 0000000000000000 001	0x02800001
Read RATE_Y2	RATE_Y2	0 0 00001011 0 0 0 0000000000000000 011	0x02C00003
Read RATE_Z2	RATE_Z2	0 0 00001100 0 0 0 0000000000000000 110	0x03000006
Read ACC_X2	ACC_X2	0 0 00001101 0 0 0 0000000000000000 100	0x03400004
Read ACC_Y2	ACC_Y2	0 0 00001110 0 0 0 0000000000000000 010	0x03800002
Read ACC_Z2	ACC_Z2	0 0 00001111 0 0 0 0000000000000000 000	0x03C00000
Read Temperature	TEMP	0 0 00010000 0 0 0 0000000000000000 100	0x04000004
Read STAT_SUM	STAT_SUM	0 0 00010100 0 0 0 0000000000000000 111	0x05000007
Read STAT_SUM_SAT	STAT_SUM_SAT	0 0 00010101 0 0 0 0000000000000000 101	0x05400005
Read STAT_COM	STAT_COM	0 0 00010110 0 0 0 0000000000000000 011	0x05800003
Read STAT_RATE_COM	STAT_RATE_COM	0 0 00010111 0 0 0 0000000000000000 001	0x05C00001
Read STAT_RATE_X	STAT_RATE_X	0 0 00011000 0 0 0 0000000000000000 010	0x06000002

Command	Register	SPI Binary Frame	SPI Hex frame
Read STAT_RATE_Y	STAT_RATE_Y	0 0 00011001 0 0 0 0000000000000000 000	0x06400000
Read STAT_RATE_Z	STAT_RATE_Z	0 0 00011010 0 0 0 0000000000000000 110	0x06800006
Read STAT_ACC_X	STAT_ACC_X	0 0 00011011 0 0 0 0000000000000000 100	0x06C00004
Read STAT_ACC_Y	STAT_ACC_Y	0 0 00011100 0 0 0 0000000000000000 001	0x07000001
Read STAT_ACC_Z	STAT_ACC_Z	0 0 00011101 0 0 0 0000000000000000 011	0x07400003

6.6.2 48-bit mode operations

The SPI binary frame is constructed as follows:
(TA9 TA8 TA[7:0] RW 0 FrTyp AE[6:0] DATA[19:0] CRC8)

Table 23 48-bit mode operations and their equivalent SPI frames

Command	Register	SPI Binary Frame	SPI Hex frame
EOI	CTRL_MODE	0 0 00110101 1 0 1 0000000 00000000000000000011 10001101	0x0D680000038D
EN_SENSOR	CTRL_MODE	0 0 00110101 1 0 1 0000000 00000000000000000001 11010011	0x0D68000001D3
Set LPF0 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 1 0000000 00000000000000000000 00010110	0x096800000016
Set LPF0 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 1 0000000 00000000000000000000 00100000	0x09A800000020
Set LPF1 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 1 0000000 00000000000001001001 10001000	0x096800004988
Set LPF1 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 1 0000000 00000000000001001001 10111110	0x09A8000049BE
Set LPF2 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 1 0000000 00000000000010010010 00000101	0x096800009205
Set LPF2 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 1 0000000 00000000000010010010 00110011	0x09A800009233
Set LPF3 to RATE_XYZ	CTRL_FILT_RATE	0 0 00100101 1 0 1 0000000 00000000000011011011 10011011	0x09680000DB9B
Set LPF3 to ACC_XYZ1/2	CTRL_FILT_ACC12	0 0 00100110 1 0 1 0000000 00000000000011011011 10101101	0x09A80000DBAD
Set RATE Dynamic Range to ±315°/s	CTRL_RATE	0 0 00101000 1 0 1 0000000 00000010010000000000 10100110	0x0A28002400A6
Set ACC Dynamic Range to ±80m/s^2	CTRL_ACC12	0 0 00101001 1 0 1 0000000 00000010010000000000 01010001	0x0A6800240051
Read RATE LPF setting	CTRL_FILT_RATE	0 0 00100101 0 0 1 0000000 00000000000000000000 11111010	0x0948000000FA
Read ACC LPF setting	CTRL_FILT_ACC12	0 0 00100110 0 0 1 0000000 00000000000000000000 11001100	0x0988000000CC
Read RATE_X1	RATE_X1	0 0 00000001 0 0 1 0000000 00000000000000000000 10101100	0x0048000000AC
Read RATE_Y1	RATE_Y1	0 0 00000010 0 0 1 0000000 00000000000000000000 10011010	0x00880000009A
Read RATE_Z1	RATE_Z1	0 0 00000011 0 0 1 0000000 00000000000000000000 01101101	0x00C80000006D
Read ACC_X1	ACC_X1	0 0 00000100 0 0 1 0000000 00000000000000000000 11111001	0x0108000000F6
Read ACC_Y1	ACC_Y1	0 0 00000101 0 0 1 0000000 00000000000000000000 00000001	0x014800000001
Read ACC_Z1	ACC_Z1	0 0 00000110 0 0 1 0000000 00000000000000000000 00110111	0x018800000037
Read ACC_X3	ACC_X3	0 0 00000111 0 0 1 0000000 00000000000000000000 11000000	0x01C8000000C0
Read ACC_Y3	ACC_Y3	0 0 00001000 0 0 1 0000000 00000000000000000000 00101110	0x02080000002E
Read ACC_Z3	ACC_Z3	0 0 00001001 0 0 1 0000000 00000000000000000000 11011001	0x0248000000D9
Read RATE_X2	RATE_X2	0 0 00001010 0 0 1 0000000 00000000000000000000 11101111	0x0288000000EF
Read RATE_Y2	RATE_Y2	0 0 00001011 0 0 1 0000000 00000000000000000000 00011000	0x02C800000018
Read RATE_Z2	RATE_Z2	0 0 00001100 0 0 1 0000000 00000000000000000000 10000011	0x030800000083

Command	Register	SPI Binary Frame	SPI Hex frame
Read ACC_X2	ACC_X2	0 0 00001101 0 0 1 0000000 00000000000000000000 01110100	0x034800000074
Read ACC_Y2	ACC_Y2	0 0 00001110 0 0 1 0000000 00000000000000000000 01000010	0x038800000042
Read ACC_Z2	ACC_Z2	0 0 00001111 0 0 1 0000000 00000000000000000000 10110101	0x03C8000000B5
Read Temperature	TEMP	0 0 00010000 0 0 1 0000000 00000000000000000000 10110001	0x0408000000B1
Read STAT_SUM	STAT_SUM	0 0 00010100 0 0 1 0000000 00000000000000000000 00011100	0x05080000001C
Read STAT_SUM_SAT	STAT_SUM_SAT	0 0 00010101 0 0 1 0000000 00000000000000000000 11101011	0x0548000000EB
Read STAT_COM	STAT_COM	0 0 00010110 0 0 1 0000000 00000000000000000000 11011101	0x0588000000DD
Read STAT_RATE_COM	STAT_RATE_COM	0 0 00010111 0 0 1 0000000 00000000000000000000 00101010	0x05C80000002A
Read STAT_RATE_X	STAT_RATE_X	0 0 00011000 0 0 1 0000000 00000000000000000000 11000100	0x0608000000C4
Read STAT_RATE_Y	STAT_RATE_Y	0 0 00011001 0 0 1 0000000 00000000000000000000 00110011	0x064800000033
Read STAT_RATE_Z	STAT_RATE_Z	0 0 00011010 0 0 1 0000000 00000000000000000000 00000101	0x068800000005
Read STAT_ACC_X	STAT_ACC_X	0 0 00011011 0 0 1 0000000 00000000000000000000 11110010	0x06C8000000F2
Read STAT_ACC_Y	STAT_ACC_Y	0 0 00011100 0 0 1 0000000 00000000000000000000 01101001	0x070800000069
Read STAT_ACC_Z	STAT_ACC_Z	0 0 00011101 0 0 1 0000000 00000000000000000000 10011110	0x07480000009E

7 Register definition

7.1 Register map user guide

7.1.1 Value and address formats

Several value formats are used in this data sheet. These are described in table below.

Table 24 Value formats

Decimal	5-bit decimal	5-bit signed hex	5-bit binary
13	13d	0Dh	5b01101
-13	-13d	13h	5b10011

All essential register content of SCH16T ASIC is mirrored to public memory banks listed below.

15h0000
15h0010
15h0020
15h0030

Detailed register content is explained in the next chapter. register address is a 4-bit offset within a memory bank. final public address is formed by adding address offset to public bank address, for example:
STAT_SUM register:
- Bank address: 15h0010
- Address offset 4h4
- Public Address: 15h0010 + 4h4 = 15h0014

7.1.2 Register map overview

Memory banks, address offsets and data widths can be seen in table below.

Green: Data registers
Red: Counters
Blue: Status registers
Orange: Control registers
Purple: Misc registers

Table 25 Register map overview

Adress	15h0000	Data width	15h0010	Data width	15h0020	Data width	15h0030	Data width
4h0	Reserved	-	TEMP	16-bit	Reserved	-	Reserved	-
4h1	RATE_X1	20-bit	RATE_DCNT	12-bit	Reserved	-	Reserved	-
4h2	RATE_Y1	20-bit	ACC_DCNT	14-bit	Reserved	-	Reserved	-
4h3	RATE_Z1	20-bit	FREQ_CNTR	16-bit	Reserved	-	CTRL_USER_IF	16-bit
4h4	ACC_X1	20-bit	STAT_SUM	16-bit	Reserved	-	CTRL_ST	13-bit
4h5	ACC_Y1	20-bit	STAT_SUM_SAT	16-bit	CTRL_FILT_RATE	9-bit	CTRL_MODE	4-bit
4h6	ACC_Z1	20-bit	STAT_COM	16-bit	CTRL_FILT_ACC12	9-bit	CTRL_RESET	4-bit
4h7	ACC_X3	20-bit	STAT_RATE_COM	16-bit	CTRL_FILT_ACC3	9-bit	SYS_TEST	16-bit
4h8	ACC_Y3	20-bit	STAT_RATE_X	16-bit	CTRL_RATE	15-bit	SPARE_1	16-bit
4h9	ACC_Z3	20-bit	STAT_RATE_Y	16-bit	CTRL_ACC12	15-bit	SPARE_2	16-bit
4hA	RATE_X2	20-bit	STAT_RATE_Z	16-bit	CTRL_ACC3	3-bit	SPARE_3	16-bit
4hB	RATE_Y2	20-bit	STAT_ACC_X	16-bit	Reserved	-	ASIC_ID	12-bit
4hC	RATE_Z2	20-bit	STAT_ACC_Y	16-bit	Reserved	-	COMP_ID	16-bit

Adress	15h0000	Data width	15h0010	Data width	15h0020	Data width	15h0030	Data width
4hD	ACC_X2	20-bit	STAT_ACC_Z	16-bit	Reserved	-	SN_ID1	16-bit
4hE	ACC_Y2	20-bit	STAT_SYNC_ACTIVE	12-bit	Reserved	-	SN_ID2	16-bit
4hF	ACC_Z2	20-bit	STAT_INFO	9-bit	Reserved	-	SN_ID3	16-bit

7.2 Sensor data block

SPI frame bit D1/D0 is specified according to Safe SPI standard.
The sensor data bit D identifies if SPI response frame contains sensor data (i.e., identifies response frame format).
D=0: no sensor data, e.g., status data or read back of configuration data
D=1: sensor data

Table 26 Overview of sensor data block

Register Name	Register Description	R/RW	Public addr
RATE_X1	Output, x-axis gyroscope, interpolation, common low pass filter with RATE_X2	R	15h0001, D1
RATE_Y1	Output, y-axis gyroscope, interpolation, common low pass filter with RATE_Y2	R	15h0002, D1
RATE_Z1	Output, z-axis gyroscope, interpolation, common low pass filter with RATE_Z2	R	15h0003, D1
ACC_X1	Output, x-axis accelerometer, interpolation, common low pass filter with ACC_X2	R	15h0004, D1
ACC_Y1	Output, y-axis accelerometer, interpolation, common low pass filter with ACC_Y2	R	15h0005, D1
ACC_Z1	Output, z-axis accelerometer, interpolation, common low pass filter with ACC_Z2	R	15h0006, D1
ACC_X3	Output, x-axis accelerometer, auxiliary signal path with interpolation and individually configurable low pass filter setting.	R	15h0007, D1
ACC_Y3	Output, y-axis accelerometer, auxiliary signal path with interpolation and individually configurable low pass filter setting.	R	15h0008, D1
ACC_Z3	Output, z-axis accelerometer, auxiliary signal path with interpolation and individually configurable low pass filter setting.	R	15h0009, D1
RATE_X2	Output, x-axis gyroscope, configurable decimation filter, common low pass filter with RATE_X1	R	15h000A, D1
RATE_Y2	Output, y-axis gyroscope, configurable decimation filter, common low pass filter with RATE_Y1	R	15h000B, D1
RATE_Z2	Output, z-axis gyroscope, configurable decimation filter, common low pass filter with RATE_Z1	R	15h000C, D1
ACC_X2	Output, x-axis accelerometer, configurable decimation filter, common low pass filter with ACC_X1	R	15h000D, D1
ACC_Y2	Output, y-axis accelerometer, configurable decimation filter, common low pass filter with ACC_Y1	R	15h000E, D1
ACC_Z2	Output, z-axis accelerometer, configurable decimation filter, common low pass filter with ACC_Z1	R	15h000F, D1
TEMP	Output, temperature sensor	R	15h0010, D1

7.2.1 Example of angular rate data conversion

Interpolated output of Rate X is used as example. Data is in 2's complement format.

16-bit mode
In 16-bit mode, default sensitivity is 100 LSB/(°/s)
If Rate X register (15h0001) read result is Rate X = 802**FFE0**7h, content is converted to angular rate as follows:
- 802h = 1 0 0 0000 0001 0b (contains D bit, address bits and first Status bit)
- FFE0h = 1111 1111 1110 0000b (Rate X register content)
- FFE0h in 2's complement format = -32d
- Angular rate = -32 LSB/sensitivity = -32 LSB/ (100 LSB/(°/s)) = -0.32 °/s
- 7h = CRC of 802FFE0h

20-bit mode
In 20-bit mode, default sensitivity is 1600 LSB/(°/s)
If Rate X register (15h0001) read result is Rate X =80200**FFE00**ADh, content is converted to angular rate as follows:
- 80200h = 1 0 0 0000 0001 0 0 00 0000 0b (contains D-bit, address-, status- and DCNT bits and one empty bit)
- FFE00h = 1111 1111 1110 0000 0000b (Rate X register content)
- FFE00h in 2's complement format = -512d
- Angular rate = -512 LSB/sensitivity = -512 LSB/ (1600 LSB/(°/s)) = -0.32 °/s
- ADh = CRC of 80200FFE00h

7.2.2 Example of acceleration data conversion

Interpolated output of ACC Y is used as example. Data is in 2's complement format.

16-bit mode
In 16-bit mode, default sensitivity is 200 LSB/(m/s^2)
If ACC Y register (15h0005) read result is ACC Y= 80A**00DC**6h, content is converted to acceleration as follows:
- 80Ah = 1 0 0 0000 0101 0b (contains D bit, address bits and first Status bit)
- 00DCh =0000 0000 1101 1100b (ACC Y register content)
- 00DCh in 2's complement format = 220d
- Acceleration = 220 LSB/sensitivity = 220 LSB/ (200 LSB/(m/s^2)) ≈ 1.1 m/s^2
- 6h = CRC of 80A00DC0h

20-bit mode
In 20-bit mode, default sensitivity is 3200 LSB/(m/s^2)
If ACC Y register (15h0005) read result is ACC Y= 80A00**00DC0**DBh, content is converted to acceleration as follows:
- 80A00h = 1 0 0 0000 0101 0 0 00 0000 0b (contains D-bit, address-, status- and DCNT bits and one empty bit)
- 00DC0h =0000 0000 1101 1100 0000b (ACC Y register content)
- 00DC0h in 2's complement format = 3520d
- Acceleration= 3520 LSB/sensitivity = 3520 LSB/ (3200 LSB/(m/s^2)) ≈ 1.1 m/s^2
- DBh = CRC of 80A00DC000h

7.2.3 Example of temperature data conversion

16-bit mode

Temperature signal sensitivity is 100 LSB/°C

If TEMP register (15h0010) read result is TEMP = 820**00DC**5h, content is converted to temperature as follows:

- 820h = 1 0 0 0001 0000 0b (contains D bit, address bits and first Status bit)
- 00DCh =0000 0000 1101 1100b (TEMP register content)
- 00DCh in 2's complement format = 220d
- Temperature= 220 LSB/sensitivity = 220 LSB/ (100 LSB/°C) = 2.2°C
- 5h = CRC of 82000DC0h

20-bit mode

The temperature data is always 16-bit wide. In 20-bit mode, this needs to be taken into account. The user has two options:

1. Change frame type for temperature register read to 32-bit by changing FT bit of previous MOSI frame from 1 to 0. Then, convert TEMP data as explained in 16-bit mode.
2. Read TEMP register in 20-bit mode. As data is only 16-bits wide, the remaining LSBs will be all zeroes and they need to be discarded. After that, register content can be converted in similar manner as explained in 16-bit mode.

If TEMP register (15h0010) read result is TEMP = 82000**00DC0**EAh, content is converted to temperature (°C) as follows:

- 82000h = 1 0 0 0001 0000 0 0 00 0000 0b (contains D-bit, address-, status- and DCNT bits and one empty bit)
- Discard last byte (**0**h).
- 00DCh =0000 0000 1101 1100b (TEMP register content)
- 00DCh in 2's complement format = 220d
- Temperature= 220 LSB/sensitivity = 220 LSB/ (100 LSB/°C) = 2.2°C
- EAh = CRC of 82000DC000h

7.3 Sensor status block

Table 27 Overview of sensor status block

Register Name	Register Description	R/RW	Public addr
RATE_DCNT	Data counter for RATE_XYZ2	R	15h0011, D0
ACC_DCNT	Data counter for ACC_XYZ	R	15h0012, D0
FREQ_CNTR	Frequency / sample time counter	R	15h0013, D0
STAT_SUM	Status summary for non-saturation related flags	R	15h0014, D0
STAT_SUM_SAT	Status summary for saturation flags	R	15h0015, D0
STAT_COM	Common Status flags, incl. TEMP, 1st level status register	R	15h0016, D0
STAT_RATE_COM	Common gyro status flags (primary channel), 1st level status register	R	15h0017, D0
STAT_RATE_X	RATE_X status flags, 1st level status register	R	15h0018, D0
STAT_RATE_Y	RATE_Y status flags, 1st level status register	R	15h0019, D0
STAT_RATE_Z	RATE_Z status flags, 1st level status register	R	15h001A, D0
STAT_ACC_X	ACC_X status flags, 1st level status register	R	15h001B, D0
STAT_ACC_Y	ACC_Y status flags, 1st level status register	R	15h001C, D0
STAT_ACC_Z	ACC_Z status flags, 1st level status register	R	15h001D, D0
STAT_SYNC_ACTIVE	Status of SYNC on each channel	R	15h001E, D0
STAT_INFO	Low power mode indications	R	15h001F, D0
Reserved	Reserved	R	15h0020, D0

7.3.1 Data counters

Table 28 Data counter registers

Register Name	Register Description	R/RW	Public addr
RATE_DCNT	Data counter for RATE_XYZ2 output channel	R	15h0011, D0
ACC_DCNT	Data Counter for ACC_XYZ2 output channel	R	15h0012, D0

Table 29 RATE_DCNT register bit description

Bit Name	Bit Description	Bits	Reset Value
RATE_Z_DCNT	4-bit data counter for RATE_Z output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[11:8]	4b0000
RATE_Y_DCNT	4-bit data counter for RATE_Y output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[7:4]	4b0000
RATE_X_DCNT	4-bit data counter for RATE_X output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[3:0]	4b0000

Table 30 ACC_DCNT register bit description

Bit Name	Bit Description	Bits	Reset Value
ACC_Z_DCNT	4-bit data counter for ACC_Z output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[11:8]	4b0000
ACC_Y_DCNT	4-bit data counter for ACC_Y output. Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[7:4]	4b0000
ACC_X_DCNT	4-bit data counter for ACC_X output Data counter value is updated (+1) when a new sample is available from corresponding RATE/ACC channel. When counter reaches 4d15, it rolls back to zero.	[3:0]	4b0000

7.3.2 Frequency counter / timestamp

Table 31 Frequency counter register

Register Name	Register Description	R/RW	Public addr
FREQ_CNTR	Frequency / sample time counter	R	15h0013, D0

Table 32 FREQ_CNTR register bit description

Bit Name	Bit Description	Bits
FREQ_CNTR_BIT	14-bit counter. Counter value is updated (+1) with every rising edge of master clock. If counter is not reset and it reaches 14d16383 it rolls back to zero.	[13:0]

7.3.3 Status summary

Table 33 Status summary register

Register Name	Register Description	Public addr
STAT_SUM	Status Summary for non-saturation related flags	15h0014, D0

Table 34 STAT_SUM register bit description

Bit Name	Bit Description	Bits	Normal operation value
Reserved	Reserved	[15:8]	8b11111111
STAT_SUM_CMN	Common Status	[7:7]	1b1
STAT_SUM_RATE_X	RATE_X Status	[6:6]	1b1
STAT_SUM_RATE_Y	RATE_Y Status	[5:5]	1b1
STAT_SUM_RATE_Z	RATE_Z Status	[4:4]	1b1
STAT_SUM_ACC_X	ACC_X Status	[3:3]	1b1
STAT_SUM_ACC_Y	ACC_Y Status	[2:2]	1b1
STAT_SUM_ACC_Z	ACC_Z Status	[1:1]	1b1
SUM_STAT_INIT_RDY	Initialization Ready	[0:0]	1b1

7.3.4 Saturation status summary

Table 35 Saturation summary register

Register Name	Register Description	Public addr
STAT_SUM_SAT	Status summary for saturation flags	15h0015, D0

Table 36 STAT_SUM_SAT register bit description

Bit Name	Bit Description	Bits	Normal operation value
Reserved	Reserved	[15:15]	1b1
STAT_SUM_SAT_RATE_X1	Saturation status for output RATE_X1	[14:14]	1b1
STAT_SUM_SAT_RATE_Y1	Saturation status for output RATE_Y1	[13:13]	1b1
STAT_SUM_SAT_RATE_Z1	Saturation status for output RATE_Z1	[12:12]	1b1
STAT_SUM_SAT_ACC_X1	Saturation status for output ACC_X1	[11:11]	1b1
STAT_SUM_SAT_ACC_Y1	Saturation status for output ACC_Y1	[10:10]	1b1
STAT_SUM_SAT_ACC_Z1	Saturation status for output ACC_Z1	[9:9]	1b1
STAT_SUM_SAT_ACC_X3	Saturation status for output ACC_X3	[8:8]	1b1
STAT_SUM_SAT_ACC_Y3	Saturation status for output ACC_Y3	[7:7]	1b1
STAT_SUM_SAT_ACC_Z3	Saturation status for output ACC_Z3	[6:6]	1b1
STAT_SUM_SAT_RATE_X2	Saturation status for output RATE_X2	[5:5]	1b1
STAT_SUM_SAT_RATE_Y2	Saturation status for output RATE_Y2	[4:4]	1b1
STAT_SUM_SAT_RATE_Z2	Saturation status for output RATE_Z2	[3:3]	1b1
STAT_SUM_SAT_ACC_X2	Saturation status for output ACC_X2	[2:2]	1b1
STAT_SUM_SAT_ACC_Y2	Saturation status for output ACC_Y2	[1:1]	1b1
STAT_SUM_SAT_ACC_Z2	Saturation status for output ACC_Z2	[0:0]	1b1

7.3.5 Common status

Table 37 Common status register

Register Name	Register Description	Public addr
STAT_COM	Common Status flags,	15h0016, D0

Table 38 STAT_COM register bit description

Bit Name	Bit Description	Bits	Normal operation value
Reserved	Reserved	[15:11]	5b11111
MCLK_OK	Status of ASIC master clock.	[10:10]	1b1
DUAL_CLOCK_OK	Clock Reference status flag	[9:9]	1b1
DSP_OK	Register content integrity status flag	[8:8]	1b1
SVM_OK	SVM Self-test status flag	[7:7]	1b1
HV_CP_OK	HV Charge Pump status flag	[6:6]	1b1
SUPPLY_OK	Voltage supply status flag	[5:5]	1b1
TEMP_OK	Temperature sensor channel status flag	[4:4]	1b1
NMODE_OK	Normal Mode status flag	[3:3]	1b1

Bit Name	Bit Description	Bits	Normal operation value
NVM_STS_OK	NVM Start-up Self-test status flag	[2:2]	1b1
CMN_STS_OK	Start-up Self-test status for TEMP and common digital blocks.	[1:1]	1b1
CMN_STS_RDY	Start-up Self-test ready for TEMP and common digital blocks.	[0:0]	1b1

7.3.6 Gyroscope common status

Table 39 Gyroscope common status register

Register Name	Register Description	Public addr
STAT_RATE_COM	Common gyro status flags (primary channel)	15h0017, D0

Table 40 STAT_RATE_COM register bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:8]	8b11111111
PRI_AGC_OK	Gyro primary loop status	[7:7]	1b1
GYRO_PRI_OK	Gyro primary loop status	[6:6]	1b1
PRI_START_OK	Gyro primary loop start-up status	[5:5]	1b1
GYRO_HV_OK	Gyro High Voltage status	[4:4]	1b1
RESERVED	Reserved	[3:3]	1b1
GYRO_SD_STS_OK	Gyro Shield Detection Start-up Self-test status	[2:2]	1b1
GYRO_BOND_STS_OK	Gyro Bond wire Start-up Self-test status	[1:1]	1b1
GYRO_STS_RDY_OK	Gyro Start-up Self-test ready status flag	[0:0]	1b1

7.3.7 Gyroscope status XYZ

Table 41 Gyroscope status registers

Register Name	Register Description	R/RW	Public addr
STAT_RATE_X	RATE_X status flags	R	15h0018, D0
STAT_RATE_Y	RATE_Y status flags	R	15h0019, D0
STAT_RATE_Z	RATE_Z status flags	R	15h001A, D0

Table 42 STAT_RATE_X register bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:10]	6b111111
RATE_DEC_X_SAT_OK	Decimated Rate (X2) Output saturation.	[9:9]	1b1
RATE_INTP_X_SAT_OK	Interpolated Rate (X1) Output saturation.	[8:8]	1b1
RESERVED	Reserved	[7:7]	1b1
RATE_X_STC_DIG_OK	Status of RATE X Digital Continuous Self-test	[6:6]	1b1
RATE_X_STC_ANA_OK	Status of RATE X Analog Continuous Self-test	[5:5]	1b1
RATE_X_QC_OK	Status of rate X signal	[4:4]	1b1
RESERVED	Reserved	[3:2]	1b1
RESERVED	Reserved	[1:1]	1b1
RESERVED	Reserved	[0:0]	1b1

Table 43 STAT_RATE_Y register bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:10]	61b111111
RATE_DEC_Y_SAT_OK	Decimated Rate (Y2) Output saturation.	[9:9]	1b1
RATE_INTP_Y_SAT_OK	Interpolated Rate (Y1) Output saturation.	[8:8]	1b1
RESERVED	Reserved	[7:7]	1b1
RATE_Y_STC_DIG_OK	Status of RATE Y Digital Continuous Self-test	[6:6]	1b1

Bit Name	Bit Description	Bits	Normal operation value
RATE_Y_STC_ANA_OK	Status of RATE Y Analog Continuous Self-test	[5:5]	1b1
RATE_Y_QC_OK	Status of rate Y signal	[4:4]	1b1
RESERVED	Reserved	[3:2]	1b1
RESERVED	Reserved	[1:1]	1b1
RESERVED	Reserved	[0:0]	1b1

Table 44 STAT_RATE_Z register bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:10]	6b111111
RATE_DEC_Z_SAT_OK	Decimated Rate (Z2) Output saturation.	[9:9]	1b1
RATE_INTP_Z_SAT_OK	Interpolated Rate (Z1) Output saturation.	[8:8]	1b1
RESERVED	Reserved	[7:7]	1b1
RATE_Z_STC_DIG_OK	Status of RATE Z Digital Continuous Self-test	[6:6]	1b1
RATE_Z_STC_ANA_OK	Status of RATE Z Analog Continuous Self-test	[5:5]	1b1
RATE_Z_QC_OK	Status of rate Z signal	[4:4]	1b1
RESERVED	Reserved	[3:2]	1b1
RESERVED	Reserved	[1:1]	1b1
RESERVED	Reserved	[0:0]	1b1

7.3.8 Accelerometer status XYZ

Table 45 Accelerometer status registers

Register Name	Register Description	R/RW	Public addr
STAT_ACC_X	ACC_X status flags	R	15h001B, D0
STAT_ACC_Y	ACC_Y status flags	R	15h001C, D0
STAT_ACC_Z	ACC_Z status flags	R	15h001D, D0

Table 46 STAT_ACC_X register bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:11]	5b11111
ACC_X3_SAT_OK	ACC_X3 output saturation.	[10:10]	1b1
ACC_X_DEC_SAT_OK	Decimated ACC (X2) output saturation.	[9:9]	1b1
ACC_X_INTP_SAT_OK	Interpolated ACC (X1) output saturation.	[8:8]	1b1
ACC_X_STC_DIG_OK	Accelerometer X Axis Continuous Self-test status 4	[7:7]	1b1
ACC_X_STC_TCAP_OK	Accelerometer X Axis Test-Cap Continuous Self-test status	[6:6]	1b1
ACC_X_STC_SDD_OK	Accelerometer X Axis Continuous Self-test status 2	[5:5]	1b1
ACC_X_STC_N_OK	Accelerometer X Axis Tone Continuous Self-test status	[4:4]	1b1
RESERVED	Reserved	[3:3]	1b1
ACC_X_SD_STS_OK	Accelerometer X Axis Shield Detection Start-up Self-test status	[2:2]	1b1
ACC_X_STS_OK	Accelerometer X Axis Start-up Self-test status	[1:1]	1b1
ACC_X_STS_RDY_OK	Accelerometer X Axis Start-up Self-test ready	[0:0]	1b1

Table 47 STAT_ACC_Y register bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:11]	5b11111
ACC_Y3_SAT_OK	ACC_Y3 output saturation.	[10:10]	1b1
ACC_Y_DEC_SAT_OK	Decimated ACC (Y2) output saturation.	[9:9]	1b1
ACC_Y_INTP_SAT_OK	Interpolated ACC (Y1) output saturation.	[8:8]	1b1
ACC_Y_STC_DIG_OK	Accelerometer Y Axis Continuous Self-test status 4	[7:7]	1b1
ACC_Y_STC_TCAP_OK	Accelerometer Y Axis Test-Cap Continuous Self-test status	[6:6]	1b1
ACC_Y_STC_SDD_OK	Accelerometer Y Axis Continuous Self-test status 2	[5:5]	1b1
ACC_Y_STC_N_OK	Accelerometer Y Axis Tone Continuous Self-test status	[4:4]	1b1

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[3:3]	1b1
ACC_Y_SD_STS_OK	Accelerometer Y Axis Shield Detection Start-up Self-test status	[2:2]	1b1
ACC_Y_STS_OK	Accelerometer Y Axis Start-up Self-test status	[1:1]	1b1
ACC_Y_STS_RDY_OK	Accelerometer Y Axis Start-up Self-test ready	[0:0]	1b1

Table 48 STAT_ACC_Z register bit description

Bit Name	Bit Description	Bits	Normal operation value
RESERVED	Reserved	[15:11]	5b11111
ACC_Z3_SAT_OK	ACC_Z3 output saturation.	[10:10]	1b1
ACC_Z_DEC_SAT_OK	Decimated ACC (Z2) output saturation.	[9:9]	1b1
ACC_Z_INTP_SAT_OK	Interpolated ACC (Z1) output saturation.	[8:8]	1b1
ACC_Z_STC_DIG_OK	Accelerometer Z Axis Continuous Self-test status 4	[7:7]	1b1
ACC_Z_STC_TCAP_OK	Accelerometer Z Axis Test-Cap Continuous Self-test status	[6:6]	1b1
ACC_Z_STC_SDD_OK	Accelerometer Z Axis Continuous Self-test status 2	[5:5]	1b1
ACC_Z_STC_N_OK	Accelerometer Z Axis Tone Continuous Self-test status	[4:4]	1b1
RESERVED	Reserved	[3:3]	1b1
ACC_Z_SD_STS_OK	Accelerometer Z Axis Shield Detection Start-up Self-test status	[2:2]	1b1
ACC_Z_STS_OK	Accelerometer Z Axis Start-up Self-test status	[1:1]	1b1
ACC_Z_STS_RDY_OK	Accelerometer Z Axis Start-up Self-test ready	[0:0]	1b1

7.3.9 Additional status registers

Table 49 Additional status registers

Register Name	Register Description	R/RW	Public addr
STAT_SYNC_ACTIVE	Status of SYNC on each channel	R	15h001E, D0
STAT_INFO	Low power mode indications	R	15h001F, D0
Reserved	Reserved	-	15h0020, D0

Table 50 STAT_SYNC_ACTIVE register bit description

Bit Name	Bit Description	Bits	Reset value
SYNC_ACTIVE_ACC_Z2	SYNC active in output ACC_Z2	[11:11]	1b0
SYNC_ACTIVE_ACC_Y2	SYNC active in output ACC_Y2	[10:10]	1b0
SYNC_ACTIVE_ACC_X2	SYNC active in output ACC_X2	[9:9]	1b0
SYNC_ACTIVE_RATE_Z2	SYNC active in output RATE_Z2	[8:8]	1b0
SYNC_ACTIVE_RATE_Y2	SYNC active in output RATE_Y2	[7:7]	1b0
SYNC_ACTIVE_RATE_X2	SYNC active in output RATE_X2	[6:6]	1b0
SYNC_ACTIVE_ACC_Z1	SYNC active in output ACC_Z1	[5:5]	1b0
SYNC_ACTIVE_ACC_Y1	SYNC active in output ACC_Y1	[4:4]	1b0
SYNC_ACTIVE_ACC_X1	SYNC active in output ACC_X1	[3:3]	1b0
SYNC_ACTIVE_RATE_Z1	SYNC active in output RATE_Z1	[2:2]	1b0
SYNC_ACTIVE_RATE_Y1	SYNC active in output RATE_Y1	[1:1]	1b0
SYNC_ACTIVE_RATE_X1	SYNC active in output RATE_X1	[0:0]	1b0

Table 51 STAT_INFO register bit description

Bit Name	Bit Description	Bits	Reset value
Reserved	Reserved	[8:7]	1b0
Reserved	Reserved	[4:3]	1b0
Reserved	Reserved	[6:5]	1b0
ACC_LPM_OK	Accelerometer in Low Power Mode	[2:2]	1b0
RATE_LPM_OK	Gyroscope in Low Power Mode	[1:1]	1b0
SENSOR_LPM_OK	Start-up State Machine in Sensor Low Power Mode	[0:0]	1b0

7.4 Sensor control block

Table 52 Sensor control block register overview

Register Name	Register Description	R/RW	Public addr
Reserved	Reserved	RW	15h0021, D0
CTRL_FILT_RATE	RATE_XYZ Filter settings. Common filter for each axis X1/X2, Y1/Y2, Z1/Z2.	RW	15h0025, D0
CTRL_FILT_ACC12	ACC filter setting. Common filter for each ACC axis X1/X2, Y1/Y2, Z1/Z2.	RW	15h0026, D0
CTRL_FILT_ACC3	Filter setting for ACC_X3, ACC_Y3 and ACC_Z3.	RW	15h0027, D0
CTRL_RATE	Settings for Gyro post-processing decimation ratio and dynamic range	RW	15h0028, D0
CTRL_ACC12	Settings for ACC_X12, ACC_Y12, ACC_Z12 post-processing decimation ratio and dynamic range	RW	15h0029, D0
CTRL_ACC3	Settings for ACC_X3, ACC_Y3, ACC_Z3 post-processing shift dynamic range	RW	15h002A, D0
Reserved	Reserved	RW	15h002B, D0
Reserved	Reserved	RW	15h002C, D0
Reserved	Reserved	RW	15h002D, D0
Reserved	Reserved	RW	15h002E, D0
CTRL_USER_IF	User controls for SYNC, Data Ready, Strength of SPI PD/PU, slew rate ctrl, hi-speed	RW	15h0033, D0
CTRL_ST	Self-test controls (enable ST and/or request STS)	RW	15h0034, D0
CTRL_MODE	Test mode, EOI, EN_SENSOR	RW	15h0035, D0
CTRL_RESET	SPI soft reset command	RW	15h0036, D0
SYS_TEST	Empty register for testing read/write access	RW	15h0037, D0

7.4.1 Filter settings

Table 53 Filter setting registers

Register Name	Register Description	R/RW	Public addr
CTRL_FILT_RATE	RATE_XYZ Filter settings. Common filter for each axis X1/X2, Y1/Y2, Z1/Z2.	RW	15h0025, D0
CTRL_FILT_ACC12	ACC filter setting. Common filter for each ACC axis X1/X2, Y1/Y2, Z1/Z2.	RW	15h0026, D0
CTRL_FILT_ACC3	Filter setting for ACC_X3, ACC_Y3 and ACC_Z3.	RW	15h0027, D0

For detailed Filter characteristics, please refer Table 9 SCH16T Filter characteristics

Table 54 Bits for setting of filters.

Name	Bits	Nominal Cut-off Frequency (-3dB)
LPF0	'000'	68 Hz (default)
LPF1	'001'	30 Hz
LPF2	'010'	13 Hz
LPF3	'011'	280 Hz
LPF4	'100'	370 Hz
LPF5	'101'	235 Hz
LPF6	'110'	Reserved
LPF7	'111'	Bypass

Table 55 CTRL_FILT_RATE register bit description

Bit Name	Bit Description	Bits	Reset Value
FILT_SEL_RATE_Z	Filter setting for RATE_Z1 and RATE_Z2 outputs	[8:6]	3b000
FILT_SEL_RATE_Y	Filter setting for RATE_Y1 and RATE_Y2 outputs	[5:3]	3b000
FILT_SEL_RATE_X	Filter setting for RATE_X1 and RATE_X2 outputs	[2:0]	3b000

Table 56 CTRL_FILT_ACC12 register bit description

Bit Name	Bit Description	Bits	Reset Value
FILT_SEL_ACC_Z12	Filter setting for ACC_Z1 and ACC_Z2 outputs	[8:6]	3b000
FILT_SEL_ACC_Y12	Filter setting for ACC_Y1 and ACC_Y2 outputs	[5:3]	3b000
FILT_SEL_ACC_X12	Filter setting for ACC_X1 and ACC_X2 outputs	[2:0]	3b000

Table 57 CTRL_FILT_ACC3 register bit description

Bit Name	Bit Description	Bits	Reset Value
FILT_SEL_ACC_Z3	Filter setting for ACC_Z3 output	[8:6]	3b000
FILT_SEL_ACC_Y3	Filter setting for ACC_Y3 output	[5:3]	3b000
FILT_SEL_ACC_X3	Filter setting for ACC_X3 output	[2:0]	3b000

7.4.2 Dynamic range and decimation

Table 58 Registers for dynamic range and decimation setting

Register Name	Register Description	R/RW	Public addr
CTRL_RATE	Settings for Gyro post-processing decimation ratio and shift value (dynamic range)	RW	15h0028, D0
CTRL_ACC12	Settings for ACC_X12, ACC_Y12, ACC_Z12 post-processing decimation ratio and shift value (dynamic range)	RW	15h0029, D0
CTRL_ACC3	Settings for ACC_X3, ACC_Y3, ACC_Z3 post-processing shift value (dynamic range)	RW	15h002A, D0

Table 59 RATE dynamic range settings

Name	Bits	Measurement range (°/s)	Typical Electrical Headroom (°/s)	Nominal Sensitivity, 16-bit (LSB/(°/s))	Nominal Sensitivity, 20-bit (LSB/(°/s))
Undefined	'000'	-	n.a.	n.a.	n.a.
DYN1 (default)	'001'	±300	±327.5	100	1600
DYN2	'010'	±300 °/s	±327.5	100	1600
DYN3	'011'	±125 °/s	±163.75	200	3200
DYN4	'100'	±62.5 °/s	±81.875	400	6400

Table 60 ACC12 dynamic range settings

Name	Bits	Measurement Range (m/s^2)	Typical Electrical Headroom (m/s^2)	Nominal Sensitivity, 16-bit (LSB/(m/s^2))	Nominal Sensitivity, 20-bit (LSB/(m/s^2))
Undefined	'000'	-	n.a.	n.a.	n.a.
DYN1 (default)	'001'	±80	±163.4	200	3200
DYN2	'010'	±60	±81.92	400	6400
DYN3	'011'	±30	±40.96	800	12800
DYN4	'100'	±15	±20.48	1600	25600

Table 61 ACC3 dynamic range settings

Name	Bits	Measurement Range (m/s^2)	Typical Electrical Headroom (m/s^2)	Nominal Sensitivity, 16-bit (LSB/(m/s^2))	Nominal Sensitivity, 20-bit (LSB/(m/s^2))
DYN0	'000'	±80	±260	100	1600

Name	Bits	Measurement Range (m/s²)	Typical Electrical Headroom (m/s²)	Nominal Sensitivity, 16-bit (LSB/(m/s²))	Nominal Sensitivity, 20-bit (LSB/(m/s²))
(default)					
DYN1	'001'	±80	±163.4	200	3200
DYN2	'010'	±60	±81.92	400	6400
DYN3	'011'	±30	±40.96	800	12800
DYN4	'100'	±15	±20.48	1600	25600

Table 62 Decimation ratio settings

Name	Bits	Reduction Factor	Output sample rate	With Nominal F_PRIM (kHz)	f3dB (Hz)
DEC1	'000' (no decimation)	1	F_PRIM/2	11.8	NA
DEC2	'001'	2	F_PRIM/4	5.9	5975
DEC3	'010'	4	F_PRIM/8	2.95	2987
DEC4	'011'	8	F_PRIM/16	1.475	1494
DEC5	'100'	16	F_PRIM/32	0.7375	747

Table 63 RATE_CTRL Register bit description

Bit Name	Bit Description	Bits	Reset Value
DYN_RATE_XYZ1	Dynamic Range for RATE_X1/Y1/Z1 outputs.	[14:12]	3b001
DYN_RATE_XYZ2	Dynamic Range for RATE_X2/Y2/Z2 outputs.	[11:9]	3b001
DEC_RATE_Z2	Decimation ratio for RATE_Z2 output	[8:6]	3b000
DEC_RATE_Y2	Decimation ratio for RATE_Y2 output	[5:3]	3b000
DEC_RATE_X2	Decimation ratio for RATE_X2 output	[2:0]	3b000

Table 64 ACC12_CTRL Register bit description

Bit Name	Bit Description	Bits	Reset Value
DYN_ACC_XYZ1	Dynamic Range for ACC_X1/Y1/Z1 outputs.	[14:12]	3b001
DYN_ACC_XYZ2	Dynamic Range for ACC_X2/Y2/Z2 outputs.	[11:9]	3b001
DEC_ACC_Z2	Decimation ratio for ACC_Z2 output	[8:6]	3b000
DEC_ACC_Y2	Decimation ratio for ACC_Y2 output	[5:3]	3b000
DEC_ACC_X2	Decimation ratio for ACC_X2 output	[2:0]	3b000

Table 65 ACC3_CTRL Register bit description

Bit Name	Bit Description	Bits	Reset Value
DYN_ACC_XYZ3	Dynamic Range for ACC_X3/Y3/Z3 outputs.	[2:0]	3b000

7.4.3 User interface control

Table 66 User interface control register

Register Name	Register Description	R/RW	Public addr
CTRL_USER_IF	User controls for SYNC, Data Ready, Strength of SPI PD/PU, slew rate ctrl, hi-speed	RW	15h0033, D0

Table 67 CTRL_USER_IF register bit description

Bit Name	Bit Description	Bits	Reset Value
SPI_SUPPLY	SPI_MISO and DRY buffer supply range: x0 - 3.3 V+/-10% or 2.5 V+/-10% (default) 01 - 1.8 V+/-8%	[15:14]	2b00
FTREE_TDEL	Typical delay time of 1st level status clearance. When user reads data register, the associated 1st level status register is cleared after TDEL. 00 - 0.078 ms 01 - 0.625 ms 10 - 2.5 ms (default) 11 – 5 ms	[13:12]	2b10
SYNC_POL	SYNC polarity control. 0 - high active (rising edge) (default) 1 - low active (falling edge).	[11:11]	1b0
SYNC_TOC_TH	SYNC time-out counter control. Counter starts to increase value after rising edge of SYNC_DRY. When counter reaches threshold value selected by SYNC_TOC_TH, data collection is restarted. Counter is reset by falling edge of SYNC_DRY. 00 - 2^15 x MCLK (1.275...1.448 ms) 01 - 2^16 x MCLK (2.550...2.896 ms) 10 - 2^17 x MCLK (5.100...5.792 ms) 11 - 2^18 x MCLK (10.199...11.584 ms)	[10:9]	2b00
SYNC_DEC_EN	Enables data freezing for Decimated output registers and their corresponding data counter registers. Can be set both simultaneously and separately with SYNC_INTP_EN. If user enables SYNC and Data ready simultaneously, Data ready takes priority. 0 - Disable 1 - Enable	[8:8]	1b0
SYNC_INTP_EN	Enables data freezing for interpolated output registers and their corresponding data counter registers. Can be set both simultaneously and separately with SYNC_DEC_EN. If user enables SYNC and Data ready simultaneously, Data ready takes priority. 0 - Disable 1 - Enable	[7:7]	1b0
DRY_POL	Data Ready polarity control. 0 - high active (default) 1 - low active	[6:6]	1b0
DRY_DRV_EN	Enables Data ready function. Writing this bit to 1 disables SYNC function, as they cannot be used simultaneously due to shared I/O pin. 1 - DRY buffer enabled 0 - DRY buffer disabled.	[5:5]	1b0
SPI_PULL_WEAK	Control of SPI pull-down resistor strength 0- strong pull-down (default) 1 - weak pull-down.	[4:4]	1b0
MISO_SR_CTRL	MISO Slew Rate control 0 - SR control disabled without static current (fast rise/fall time ~<1ns). (Contact sales office before enabling) 1 - SR control enabled with static current (default)	[3:3]	1b1
DRY_SR_CTRL	DRY Slew Rate control 0 - SR control disabled without static current (fast rise/fall time ~<1ns). (Contact sales office before enabling) 1 - SR control enabled with static current (default)	[2:2]	1b1
DRY_HI_SPD	DRY High-Speed mode control 0 – 10 MHz mode, SafeSPI2 standard 1 – 25 MHz mode, non-standard high-speed SPI (Contact sales office before enabling)	[1:1]	1b0
MISO_HI_SPD	MISO High Speed mode control 0 – 10 MHz mode, SafeSPI2 standard 1 – 25 MHz mode, non-standard high-speed SPI. (Contact sales office before enabling)	[0:0]	1b0

7.4.4 Self-test controls

Table 68 Register for self-test controls

Register Name	Register Description	R/RW	Public addr
CTRL_ST	Self-test controls (enable ST and/or request STS)	RW	15h0034, D0

Table 69 CTRL_ST register bit description

Bit Name	Bit Description	Bits	Reset Value
Reserved	Reserved	[12:12]	1b0
RATE_Z_STC_CTRL	Enable RATE_Z continuous self-test by writing bit to '0'	[11:11]	1b1
RATE_Y_STC_CTRL	Enable RATE_Y continuous self-test by writing bit to '0'	[10:10]	1b1
RATE_X_STC_CTRL	Enable RATE_X continuous self-test by writing bit to '0'	[9:9]	1b1
ACC_Z_STC_MASK1	Mask ACC_Z continuous self-test flag (STC_N) by writing bit to '0'	[8:8]	1b1
ACC_Y_STC_MASK1	Mask ACC_Y continuous self-test flag (STC_N) by writing bit to '0'	[7:7]	1b1
ACC_X_STC_MASK1	Mask ACC_X continuous self-test flag (STC_N) by writing bit to '0'	[6:6]	1b1
ACC_Z_STC_MASK2	Mask ACC_Z continuous self-test flag (STC_SDD) by writing bit to '0'	[5:5]	1b1
ACC_Y_STC_MASK2	Mask ACC_Y continuous self-test flag (STC_SDD) by writing bit to '0'	[4:4]	1b1
ACC_X_STC_MASK2	Mask ACC_X continuous self-test flag (STC_SDD) by writing bit to '0'	[3:3]	1b1
ACC_STS_CTRL	Enable ACC start-up self-test by writing bit to '0'	[2:2]	1b1
TEMP_STS_CTRL	Enable Temperature sensor Self-test by writing bit to '0'	[1:1]	1b1
ACC_STS_REQ	Request ACC start-up self-test by writing bit to '1'. Bit is set automatically to '0' when test is over. ACC STS is performed automatically during start-up routine.	[0:0]	1b0

7.4.5 Sensor mode control and soft reset

Table 70 Registers for setting EN_SENSOR, EOI and soft reset

Register Name	Register Description	R/RW	Public addr
CTRL_MODE	EOI, EN_SENSOR	RW	15h0035, D0
CTRL_RESET	SPI soft reset command	RW	15h0036, D0

Table 71 CTRL_MODE register bit description

Bit Name	Bit Description	Bits	Reset Value
Reserved	Reserved	[3:2]	2b00
EOI_CTRL	End of Initialization, lock all R/W registers except soft reset control and SYS_TEST. This bit can only be set when there are no errors in common status.	[1:1]	1b0
EN_SENSOR	Enable RATE and ACC measurement. Write bit to '1' according to start-up sequence.	[0:0]	1b0

Table 72 CTRL_RESET register bit description

Bit Name	Bit Description	Bits	Reset Value
SOFTRESET_CTRL	Writing 4b1010 to this field generates a SPI soft reset. SPI Communication is not allowed during 2ms after SPI SOFTRESET.	[3:0]	4b0000

7.4.6 Whoami, traceability, identification, and spare registers

Table 73 Miscellaneous registers

Register Name	Register Description	R/RW	Public addr
SYS_TEST	Empty register for testing read/write access	RW	15h0037, D0
SPARE_1	Reserved	R	15h0038, D0
SPARE_2	Reserved	R	15h0039, D0
SPARE_3	Reserved	R	15h003A, D0
ASIC_ID	ASIC revision	R	15h003B, D0

Register Name	Register Description	R/RW	Public addr
COMP_ID	Component type	R	15h003C, D0
SN_ID1	Component Serial Number field 1	R	15h003D, D0
SN_ID2	Component Serial Number field 2	R	15h003E, D0
SN_ID3	Component Serial Number field 3	R	15h003F, D0

Table 74 SYS_TEST register bit description

Bit Name	Bit Description	Bits	Reset Value
SYS_TEST	16bit read/write register which can be used to check accessibility of the device, or if multiple devices are connected to the SPI bus to check if CS signals are working properly. Due to off-frame protocol, test sequence should be as follows: 1. Write data into SYS_TEST register 2. Read SYS_TEST register content 3. Issue a dummy read command to receive response from previous frame SYS_TEST register is not locked by EOI bit.	[15:0]	16b0

Table 75 ASIC_ID register bit description

Bit Name	Bit Description	Bits
ASIC_TYPE	ASIC type, always 0000 for SCH1-series products	[11:8]
ASIC_REV	ASIC major revision	[7:4]
ASIC_REV_MINOR	ASIC minor revision	[3:0]

Table 76 COMP_ID register bit description

Bit Name	Bit Description	Bits
COMP_ID	Component version. e.g., SCH16T-K01	[15:0]

The component shall be traceable by a unique electronically readable serial number.
Serial number string format: **DDDYYFHHHH H0X**

Serial number is stored in NVM registers SN_ID1, SN_ID2 and SN_ID3.

H0 is a fixed value and therefore not stored to NVM.

SN_ID1 [3:0] content corresponds to "F" part of serial number (4bit hex to string, 0...F)
Example register content: 0000, therefore 0

SN_ID1 [6:4] content corresponds to "X" part of serial number (3bit hex to string, 0…7) determining product series. For SCH16T Series the serial number ending is fixed to 1 and SN_ID1 [6:4] content is left as '0'

SN_ID2 [15:0] content corresponds to "DDDYY" part of serial number (16bit unsigned integer to decimal string, 0....65535)
Example register content: 1000 1010 0101 1111, therefore 35423

SN_ID3 [15:0] content corresponds to "HHHH" part of serial number (16bit hexadecimal running number)
Example: 0001 0100 1001 0111
0001 = 1
0100 = 4
1001 = 9
0111 = 7
, therefore 1497
Final serial number result will be 354230 1497H01

Table 77 SN_ID1 register bit description

Bit Name	Bit Description	Bits
SN_ID1	“F” part of component serial number (4-bit hex to string, 0...F) Format: DDDYYFHHHHH0X	[3:0]
SN_ID1	“X” part of component serial number (3-bit hex to string, 0…7) Format: DDDYYFHHHHH0X. For SCH16T Series the value is fixed to 0	[6:4]

Table 78 SN_ID2 register bit description

Bit Name	Bit Description	Bits
SN_ID2	“DDDYY” part of serial number (16-bit unsigned integer to decimal string, 0....65535). DDD is the production day as ordinal number from the beginning of the year and YY is production year. Format: DDDYYFHHHHH0X	[15:0]

Table 79 SN_ID3 register bit description

Bit Name	Bit Description	Bits
SN_ID3	“HHHH” part of component serial number (16-bit hexadecimal running number) Format: DDDYYFHHHHH0X	[15:0]

8 Application information

8.1 Application circuitry and external component characteristics

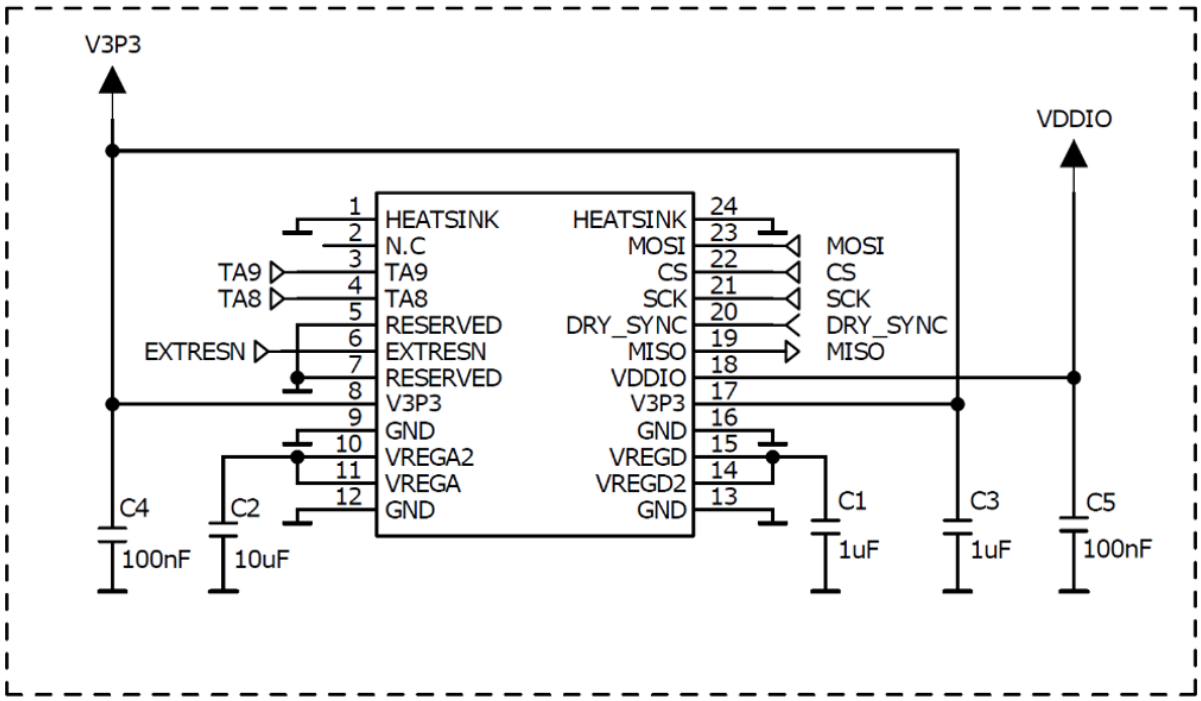


Figure 17 Application schematic

Table 80 External component description for SCH16T

Symbol	Description	Min	Nom.	Max	Unit
C1 C3	Decoupling capacitor between VREGD/VREGD2 (C1)/3p3 pin17 (C3) and GND (ESR <100 mOhm @ 1 MHz)	0.7	1	1.3	uF
C2	Decoupling capacitor between VREGA/VREGA2 and GND (ESR <100 mOhm @ 1 MHz)	4.6	10	15	uF
C4 C5	Decoupling capacitor between V3p3 pin8 (C4)/VDDIO (C5) and GND (ESR <100 mOhm @ 1 MHz)	70	100	130	nF

All GND and I/O need to be connected with below exceptions.

- TA8 and TA9 shall be connected to ground, unless application needs to communicate with multiple slaves via single Chip Select.
- If EXTRESN pin is not driven by MCU, it shall be connected to VDDIO directly or with max 20kohm PU resistor.
- DRY_SYNC shall be left floating if these features are not used.
- N.C. pin 2 shall be left floating as indicated by schematic.

8.2 General application PCB layout

A PCB layout example of the SCH16T Series component is presented in *Figure 18 Reference PCB layout*. The presented layout can be used as such or only as reference. When designing the PCB, it is advised to follow general layout guidelines below:

- Connect SMD decoupling capacitors right next to the component on top layer.
- Each ground pin should be connected to the ground directly.
- Signal lines of this component (SCH16T series) can be freely routed under the component. It is expected that signal lines of other components have also no effect on the SCH16T component, but the user is advised to verify functionality before implementation.
- Keep all routing as low resistance as possible.

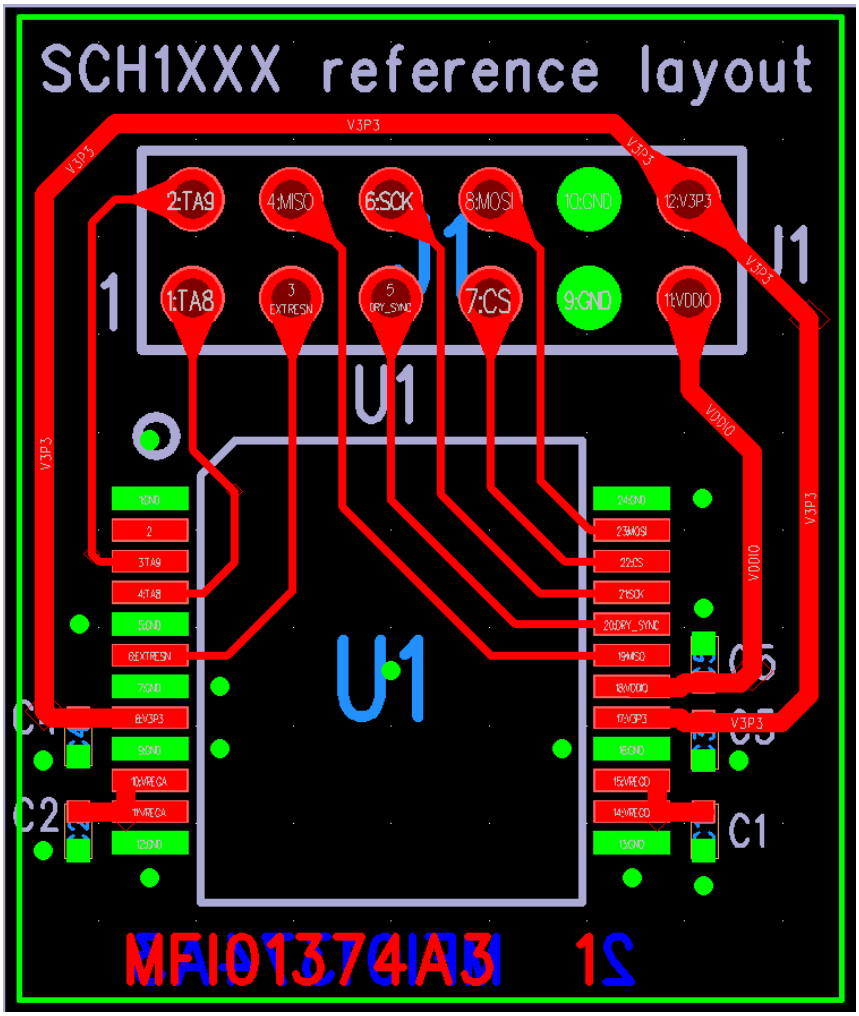


Figure 18 Reference PCB layout

For additional PCB design guidelines, please refer to the document Murata APP 10871.

9 Assembly instructions

Application PCB design, conformal coating, mechanical shocks, material selection, environment and component assembly process can impact the sensor performance. Please refer to document Murata APP 10871 for related details.